# Low-Power Receive-Electronics for a Miniature 3D Ultrasound Probe

# Low-Power Receive-Electronics for a Miniature 3D Ultrasound Probe

PROEFSCHRIFT

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. ir. K.C.A.M. Luyben
voorzitter van het College voor Promoties,
in het openbaar te verdedigen
op maandag 2 april 2012 om 12:30 uur

door

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Printed by Ipskamp Drukkers B.V., Enschede, The Netherlands.

ISBN: 978-94-6191-213-8

Financial support for the printing of this thesis was kindly provided by:

- TU Delft
- Oldelft Ultrasound B.V.

This thesis work is supported by Oldelft Ultrasound B.V., and Dutch Ministry of Economic Affairs in the framework of the program PIEKEN in de Delta, aanloopjaar 2006, project (name): “Het Hart in Drie Dimensies”.

*To my parents and Shubin*

*In memory of my grandparents*

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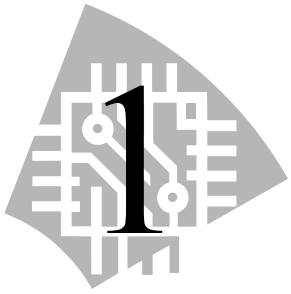
# *Introduction*




There is a clear clinical need for creating three-dimensional (3D) images of the heart. These images can give more authentic information on the 3D anatomy and function of the heart, such as the cardiac chamber volumes and the movements of the valves [1.1]. Normal imaging is done precordially. However, to obtain a more detailed view, imaging can also be performed from the esophagus. In this case, an ultrasound transound transducer is mounted in the tip of a gastroscopic tube and inserted into the esophagus to make images from the backside of the heart. This is called Trans-Esophageal Echocardiography (TEE). Now the challenge is to enable 3D TEE. We — a team consisting of Oldelft Ultrasound B.V., ErasmusMC and TU Delft is developing a miniature ultrasound probe containing a matrix piezoelectric transducer with more than 2000 elements. Since a gastroscopic tube cannot accommodate the cables needed to connect all transducer elements directly to an imaging system and so far there is no any imaging system exists with more than 256 input connections, a major challenge is to locally reduce the number of channels, while maintaining a sufficient signal-to-noise ratio (SNR). This can be achieved by using a front-end application-specific integrated circuit (ASIC) connected to the transducer that provides appropriate signal conditioning in the tip of the probe. The main goal of this

thesis work is to design such an ASIC using simple, low-power circuits, while still maintaining good image quality and to investigate the scientific problems related to this design. In addition to the electronics design, a second goal is to realize the interconnection between the matrix transducer and the ASIC.

In this introductory chapter, the basic knowledge of TEE is given. This is followed by a short discussion of the challenges and choices in designing a 3D TEE probe. It is shown that in order to reduce the channel count and enhance signal quality from the output of an ultrasound matrix transducer, smart signal processing by means of an ASIC in the tip of the probe is necessary. Meanwhile the circuits must be designed in such a way that they are compact and efficient enough to meet the stringent power and space requirements. Moreover, a new methodology is required to tackle the challenge of electrically connecting the transducer to the ASIC. Based on these challenges, the objectives and chosen design approaches are given. Finally, the thesis organization is described.

## 1.1 Trans-Esophageal Echocardiography (TEE) Basics

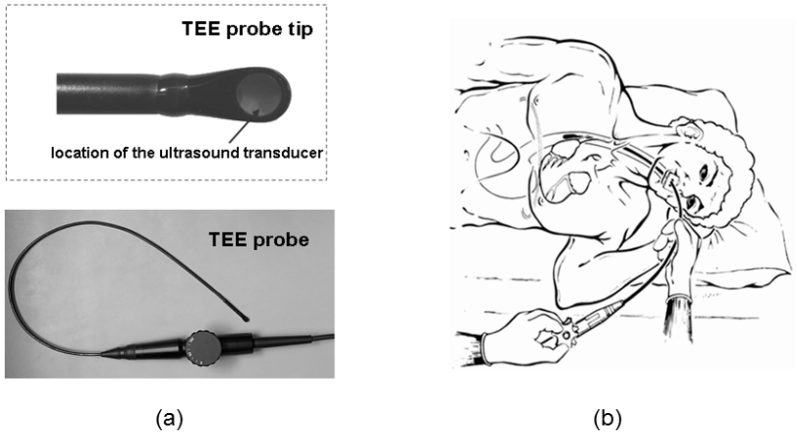



Fig. 1.1 Transesophgeal Echocardiography: (a) A TEE probe of the type 171Z- [1.5] (courtesy of Oldelft Ultrasound B.V.), (b) Use of the esophagus as a window during TEE imaging.

According to statistics from the World Health Organization (WHO) in 2011, cardiovascular diseases (CVDs) are the number-one cause of death globally [1.2]. CVDs are a group of disorders of the heart and blood vessels. In 2008, an estimated 17.3 million people died from CVDs [1.2], representing 30% of all global deaths. In order to save patients' lives, accurate diagnosis is of vital importance. For this purpose, many imaging techniques have been developed to visualize the inner structures of the heart, such as magnetic-resonance imaging (MRI), computed tomography (CT), positron emission tomography (PET), and echocardiography. Among them, echocardiography is the most popular technique, because of its low cost, non-invasive characteristic and good image quality [1.3]. Transesophageal echocardiography (TEE) is a cardiac imaging modality that uses the esophagus as the imaging window to the heart. Since the heart is directly adjacent to the wall of the esophagus, cardiac images can be obtained without strong attenuation from the ribs or the lungs, which is the case in transthoracic echocardiography (TTE) [1.4]. To enable TEE imaging, a TEE probe is indispensable (Fig. 1.1a). This probe consists of an ultrasound transducer, located in the tip of the probe, which is connected to an imaging system via a flexible gastroscopic tube. The probe is swallowed by a patient into his/her esophagus to obtain images (Fig. 1.1b).

### *Piezoelectric Ultrasound Transducers*

To make ultrasound images, signal transductions between the acoustic domain and the electrical domain are needed. In the 20th century, many physical phenomena, such as electromagnetism, electrostatic phenomenon, electric-spark, and the piezoelectric effect, have found application in ultrasound transduction [1.6]. Among them the piezoelectric effect has had a major impact on the successful development of ultrasound transducers. Many crystalline materials exhibit the piezoelectric effect, such as quartz, Rochelle salt, and the man-made lead-zirconate-titanate (PZT) ceramic. Among them, PZT is the most widely used material for ultrasound transducers [1.7].

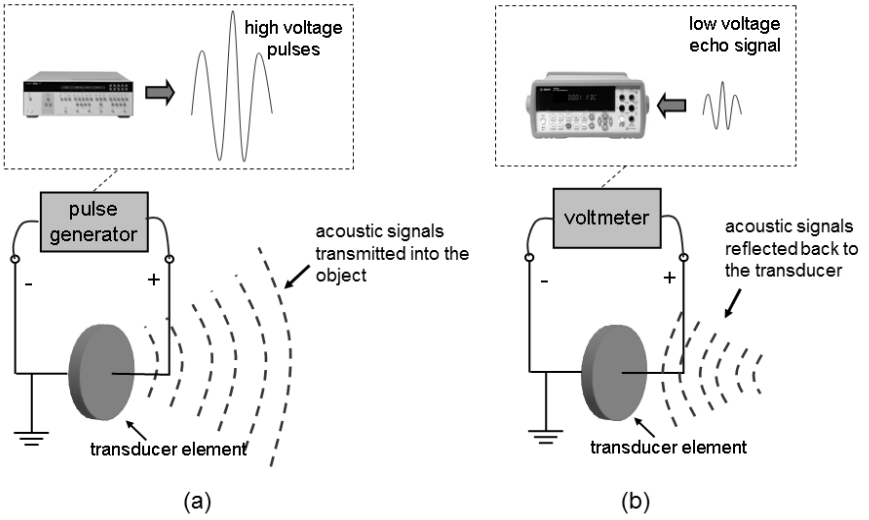



Fig. 1.2 Working mechanism of a piezoelectric ultrasound transducer: (a) transmit mode, (b) receive mode.

As shown in Fig. 1.2a, the piezoelectric ultrasound transducer is a device capable of converting energy between the electrical domain and the acoustic domain. When voltage pulses are applied across the two electrodes of the transducer, the device will oscillate at very high frequencies, thus producing sound waves in the ultrasonic range. Inversely, when an ultrasound echo signal arrives on the surface of the transducer in the form of acoustic pressure, displacements of electrical charges in the transducer occur, which leads to potential differences generated across the transducer. A piezoelectric transducer can thus play the roles of both transmitter and receiver, which is the case in many conventional ultrasound imaging systems. Piezoelectric ultrasound transducers are capable of operating at various frequencies, ranging from kHz to MHz. For medical imaging application, the transducers normally work in the frequency range of 1~40 MHz [1.8].

### *TEE Imaging Systems*

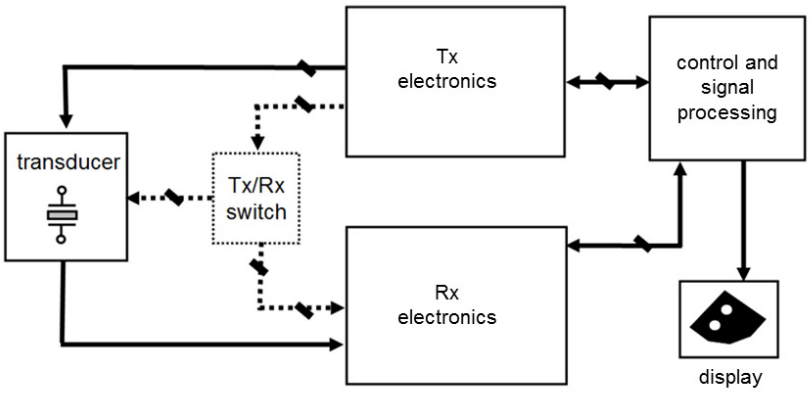



Fig. 1.3 A TEE imaging system

A typical TEE imaging system is based on the pulse-echo principle. It mainly consists of one or more ultrasound transducers with multiple elements arranged in arrays, transmit (Tx) electronics, receive (Rx) electronics, a control and signal processing module, and a display module (Fig. 1.3). Firstly, the transducer elements are excited by high-voltage pulses generated by the Tx electronics. The transducer elements convert the electrical energy into mechanical vibration. When the TEE probe is coupled to the esophageal wall against the heart, the vibration is transmitted into the heart as an acoustic wave. Depending on the acoustic impedance along the path of transmission, a certain percentage of the acoustic signals is reflected back and will hit the surfaces of transducer elements. Next, those so-called "echo" signals are picked up by the transducer elements and are converted into the electrical domain. Typical voltage levels of the echo signals in the TEE application range from several microvolts to hundreds of millivolts. These signals are further processed by Rx electronics. This processing includes amplification, time-gain-compensation (TGC) [1.9], and beamforming among multiple receive channels [1.6]. Based on the signal

strength and timing, the inner structure of the heart can be determined. Finally, an image is rendered by the display module.

If a single transducer array is used as both the transmitter and receiver, a Tx/Rx switch must be inserted between the Tx/Rx electronics (dashed line in Fig. 1.3). A protection circuit is typically also included inside the Tx/Rx switches to prevent the low-voltage Rx electronics from being damaged by the high voltage pulses. The transducer is always located in the tip of the TEE probe. In conventional TEE imaging systems, the Tx/Rx electronics and the Tx/Rx switches are located outside the probe tip. However, a new trend for 3D TEE imaging is to move these circuits (at least partially) into the probe tip [1.10].

***From 2D to 3D***

In conventional echocardiography, a one-dimensional (1D) ultrasound array is manually repositioned at several positions and angles to obtain a number of two-dimensional (2D) ultrasound images of different cross-sections of the heart. The physician mentally combines these images to form an impression of the real three-dimensional (3D) anatomy. Therefore, this method is highly subjective and depends on the skill and experience of the physician [1.11]. This issue is addressed by 3D ultrasonic imaging techniques, which have several advantages compared to conventional 2D techniques. Cardiac chamber volumes can be evaluated with more accuracy, without making assumptions on the shape of the volume [1.1]. Furthermore, cross-sectional planes and “en face” views can be reconstructed for any orientation, giving better understanding of the morphology of the various heart cavities, of defects, and of diseased valves [1.12].

A 3D dataset can be constructed from a series of 2D image planes, provided that the position and orientation of the subsequent planes are known. These image planes can be obtained by using a 1D transducer array with a mechanical scanning approach, such as stepwise translating, tilting or rotating (Fig. 1.4). Various 3D imaging techniques using 1D arrays are described in [1.13]. For TEE applications, the most common techniques use a 1D array that is rotated around its axis. A drawback of this method is that it

increases the scanning time. The acquired 3D image is not real-time, but reconstructed from data acquired at different moments in time. Moreover, the images are sensitive to imaging artifacts due to the movement of the heart [1.14].

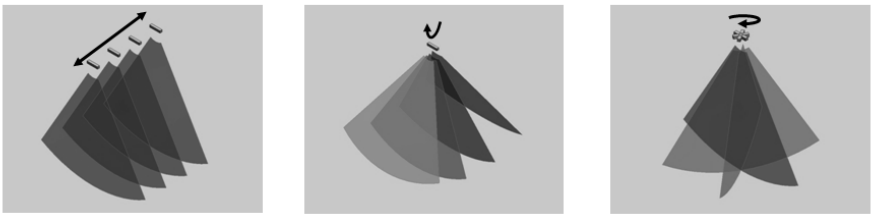
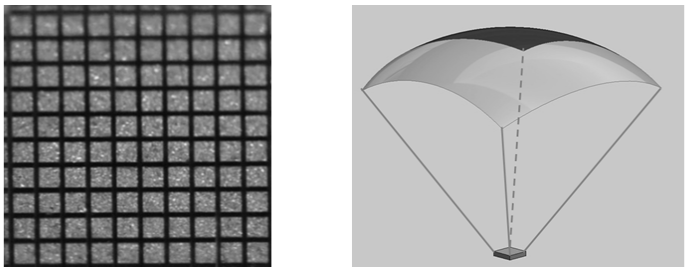



Fig. 1.4 Different methods of acquiring a 3D dataset using a 1D array: (a) translating, (b) tilting, and (c) rotating.

With a 2D transducer array (a matrix array), ultrasound beams can be emitted in any direction in a pyramidal volume. Thus, a 3D dataset can be acquired directly without the need for mechanical repositioning of the array (Fig. 1.5). At this moment, a matrix transducer for real-time 3D TEE is already commercially available (xMATRIX, Philips [1.15]). As reported in [1.16], by using an iE33 ultrasound system (Philips Medical Systems) which was equipped with a fully-sampled matrix TEE transducer of approximately 3000 elements, real-time 3D images of the mitral valve, interatrial septum, left atrium and left ventricle have been obtained with excellent image quality. However, the system is not able to scan a large volume in a single heartbeat. Instead it acquires 4~7 narrow wedges over 4~7 heartbeats to form the total volume.



(a) (b)

Fig. 1.5 Volumetric dataset acquired using a matrix transducer: (a) front-view of a matrix transducer (courtesy of Oldelft Ultrasound B.V.), (b) a volume can be imaged by a matrix transducer.

## 1.2 Design Challenges and Choices in 3D TEE

In our project, we are designing a TEE probe for real-time 3D imaging using matrix ultrasound transducers. Since the TEE probe will be inserted into the esophagus of a patient, the esophageal cavity puts a size constraint on the transducer as well as on the gastroscopic tube. To obtain 3D images with sufficient resolution, the pitch of the transducer elements should be small and the total aperture should be as large as possible. Therefore, a matrix transducer consisting of several thousands of elements is required [1.17] (more than 2000 elements in this thesis work). One of the major challenges of manufacturing a TEE probe with a matrix transducer is connecting its large number of elements to an external imaging system. Connecting each element with a separate cable is not possible because the number of cables cannot be accommodated in the shaft of the gastroscope and the tube should remain flexible: there is no imaging systems available which can handle 2000 connections. Therefore, smart signal processing is required in the tip of the probe to reduce the number of channels to the external imaging system. This can be achieved using an application-specific integrated circuit (ASIC) bonded to the matrix transducer.

In conventional ultrasound imaging systems, the same transducer works as both transmitter and receiver. As discussed in the previous section, high

voltage pulses are needed to excite transducer elements during the transmission period. To isolate the sensitive receive circuitry from these high voltage pulses and to prevent the small echo signal from being attenuated by the transmit circuitry, a Tx/Rx switch with protection circuit is mandatory. However, a typical protection circuit consists of large diodes connected back-to-back, which are usually bulky [1.6] and challenging to implement for a matrix transducer with more than 2000 elements in a limited space. Moreover, the need for high-voltage circuitry will limit the options for selecting a proper technology to implement the receiver electronics, which could be a serious drawback when keeping up with today's developments in technology.

In our design, the problem of protection is circumvented by physically separating the transducer into a transmit sub-array (Tx array) with ~128 elements and a receive sub-array (Rx array) with ~2000 elements. Two sub-arrays are placed side-by-side. The Tx array can be directly connected to the external imaging system via cables. A front-end receive ASIC is needed to interface the Rx array only. An additional advantage is that tissue harmonic imaging [1.6] (see Section 2.2.4) is possible without the need for broadband transducer elements. Furthermore, both Tx and Rx arrays can be optimized for their specific role [1.17]. The proposed block diagram of the TEE imaging system is depicted in Fig. 1.6.

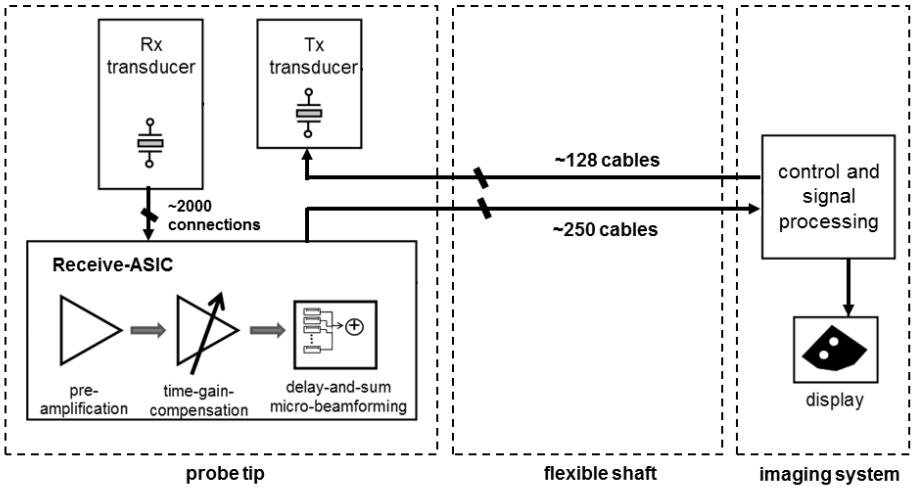



Fig. 1.6 Block diagram of the proposed TEE imaging system.

This thesis mainly focuses on the design of the receive-ASIC, which achieves channel-count reduction by applying appropriate delays to Rx-array outputs locally and coherently summing the signals from several elements. This local delay-and-sum operation is called "micro-beamforming". The ASIC should also provide proper signal pre-amplification and time-gain-compensation (TGC) to each transducer element.

For the receive-ASIC in the tip of the TEE probe, several constraints apply. One limiting factor is the space in the probe tip, which has a size of about 2 cm × 1 cm × 1 cm (length × width × height). Thus, compact circuit design and efficient use of the small space are required. To avoid overheating of the tissue, the maximum power consumption of the front-end electronics is a very critical specification as well. In a conventional TEE probe, a thermistor is employed to monitor the temperature. The system shuts down when a certain threshold temperature (42°C to 44°C) is reached [1.18]. For continuous monitoring of the heart, shut-down is undesirable. Therefore, the self-heating of the probe tip should be limited. The temperature rise in the probe tip depends on many factors, such as the power dissipation of the transducers and the electronics, and the heat-sinking capability of the wires. To obtain an estimate of the power-dissipation levels that are acceptable, the

power consumption of commercially available TEE probes in transmit mode, which is approximately 1 W to 2 W, is used as a reference. To prevent a significant increase in self-heating, we set the power budget for the receive electronics to be in the same order, and preferably not more than 1 W.

In addition to the electronics design, finding a way to connect the ASIC to the matrix ultrasound transducer is another great challenge. The major design constraints are the limited space in the probe tip, the large number of channel counts, and the processing temperature[1]. These constraints make conventional technologies, such as wire bonding technology and flip-chip technology [1.19], challenging to implement. The main research task is to develop an interconnection solution that delivers a compact structure, good electrical connectivity, etc. Moreover, the interconnection solution must fulfill the temperature requirement and be compatible with the transducer manufacturing process.

## 1.3 Objective and Chosen Approaches

The main objective of this thesis work is to tackle design challenges associated with the readout and connectivity of the receive (Rx) transducer in a TEE probe for 3D imaging. Two major design questions are:

(1) How to apply front-end signal processing using an ASIC under stringent power and space constraints?
(2) How to solve the transducer-to-ASIC interconnection issue?

The above questions are answered by the following means:

- New system approaches (Chapter 3):
  - Instead of using a conventional continuous time-gain compensation (TGC) scheme, we have chosen for a four-step discrete-gain implementation, which highly simplifies the circuit design.

[1] The processing temperature must be well below the Curie temperature of the piezoelectric material to avoid depolarization.

  - A new micro-beamforming methodology is employed to reduce the circuit-design complexity without causing significant degradation of the image quality.
- New circuit solutions (Chapters 4 & 5):
  - A low-power time-gain-compensation (TGC) amplifier has been realized by using an open-loop topology. Circuit techniques such as trans-conductance boosting using a cascaded-flipped voltage follower and Kelvin connections, are employed to improve the accuracy.
  - Analog delay lines have been designed using the pipeline-operated S/H delay architecture. This circuit topology is simple, flexible and accurate in terms of gain and timing.
  - Two micro-beamformers with different signal-summation methods have been designed. The first one employs a voltage-to-current converter and sums the signals from several channels in the current domain. The other circuit uses an elegant charge-averaging structure, which significantly reduces the power consumption.
- A new interconnection technology (Chapter 7):
  - The use of electrical conductive glue as the intermediate conductor enables an ultrasound matrix transducer to be built directly on top of an ASIC.

## 1.4 Thesis Organization

The remainder of this thesis consists of seven chapters. The thesis structure and the relationship between these chapters are shown in the flowchart below (Fig. 1.7).

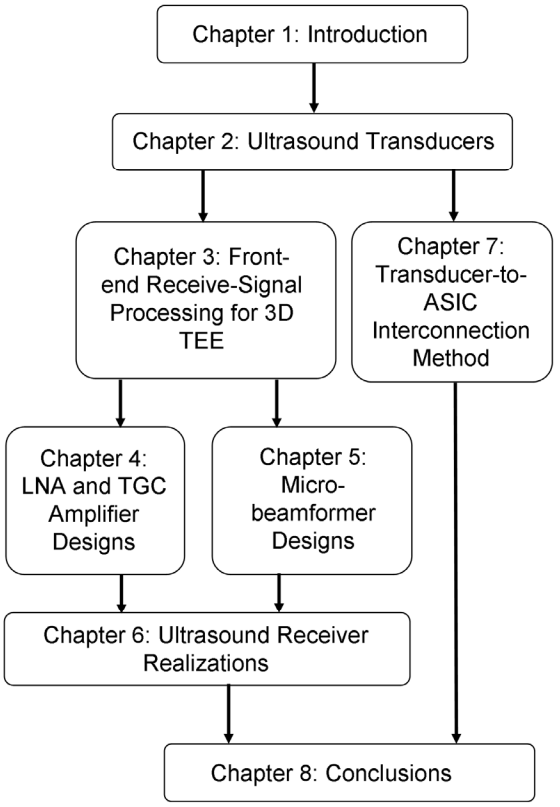



Fig. 1.7 Flowchart of the thesis organization.

Chapter 2 is an introduction to ultrasound transducers. The basic principles of operating ultrasound transducers are described. The major focus of this chapter is on the receive (Rx) transducer used for 3D TEE. Practical issues associated with this transducer such as its geometry, its electrical model, and the requirements of the associated readout-electronics design, are examined.

In Chapter 3, the system architecture of the front-end signal processing chain is given. Simplifications made to time-gain compensation (TGC) and micro-beamforming are described. The design requirements for the front-end electronics are also proposed.

In Chapters 4 and 5, designs of a low-noise amplifier, a TGC amplifier, and micro-beamforming circuits are presented. Various circuit topologies and techniques are compared, improved and optimized.

In Chapter 6, two ultrasound receivers are presented. They combine the circuit building blocks presented in Chapter 4 and Chapter 5 into complete front-end signal-processing chains. Both receivers demonstrate the effectiveness of the design approaches and deliver proofs of concepts.

In Chapter 7, a new method of electrically connecting an ultrasound matrix transducer to an ASIC is proposed and experimental results are presented.

Finally, in Chapter 8, conclusions are drawn and the main contributions of this work are summarized. Some recommendations for future research are also presented.

## 1.5 References

[1.1] R.M. Lang, V. Mor-Avi, L. Sugeng, P.S. Nieman, D.J. Sahn, "Three-dimensional echocardiography: the benefits of the additional dimension", *Journal of the American College of Cardiology*, vol. 48, no. 10, pp. 2053-2069, Nov. 2006.

[1.2] http://www.who.int/mediacentre/factsheets/fs317/en/ (2011).

[1.3] K.Y.E. Leung, *Automated Analysis of 3D Stress Echocardiography*, PhD thesis: Department of Biomedical Engineering, Erasmus University, 2009.

[1.4] E.A. Fisher, J.A. Stahl, J.H. Budd, M.E. Goldman, "Transesophageal echocardiography: procedures and clinical application", *Journal of the American College of Cardiology*, vol. 18, issue 5, pp. 1333-1348, Nov. 1991.

[1.5] Oldelft Ultrasound, "Oldelft MicroMulti TE Probe Type number 171Z-", *User Manual*, February 2010.
http://www.oldelft.nl/upload/documenten/gebruiksaanwijzingen/250m065-00a-manual-micromulti.pdf.

[1.6] R. S. C. Cobbold, *Foundations of Biomedical Ultrasound*, Oxford University Press, 2007.

[1.7] A. Arnau, *Piezoelectric Transducers and Application*, Berlin: Springer, 2008.

[1.8] M. Postema, O.H. Gilja, "Contrast-enhanced and targeted ultrasound", *World Journal of Gastroenterology*, vol. 17, no.1, pp. 28-41, 2011.

[1.9] K. Iniewski, *Medical Imaging, Principles, Detectors and Electronics*, New Jersey: John Wiley & Sons, 2009.

[1.10] V. Mor-Avi, L. Sugen, R.M. Lang, "Real-time 3-dimensional echocardiography: an integral component of the routine echocardiographic examination in adult patients", *Circulation,* vol. 119: pp. 314-29, 2009.

[1.11] A. Fenster, D. B. Downey, H. N. Cardinal, "Three-dimensional ultrasound imaging", *Physics in Medicine and Biology*, vol. 46, pp. 67-99, 2001.

[1.12] J. Roelandt, "Three-dimensional echocardiography", *Echocardiography*, part 7, pp. 603-618, London: Springer, 2009.

[1.13] B.J. Krenning, M.M. Voormolen and J.R. Roelandt, "Assessment of left venricular function by three-dimensional echocardiography", *Cardiovascular Ultrasound*, vol.1, No.12, Sept. 2003.

[1.14] A. Salustri, J. Roelandt, "Three dimensional reconstruction of the heart with rotational acquisition: methods and clinical applications", *British Heart Journal*, vol. 73, supplement 2, pp. 10-15, 1995.

[1.15] F. Taddei, L. Franceshetti, M. Signorelli, F. Prefumo, N. Fratelli, T. Frusca, C. Groli, "xMATRIX Array Transducer in Fetal Echocardiography", http://www.healthcare.philips.com/pwc_hc/main/shared/Assets/Documents/Ultrasound/Products/Campaigns/Pushing%20the%20Boundaries/xMATRIX_fetal_echo_by_Franceshetti_et_al.pdf, 2011.

[1.16] L. Sugeng, S. K. Shernan, I. S. Salgo, L. Weinert, D. Shook, J. Raman, V. Jeevanandam, F. Dupont, S. Settlemier, B. Savord, J. Fox, V. Mor-Avi, R. M. Lang, "Live 3-dimensional transesophageal echocardiography: initial

experience using the fully-sampled matrix array probe," *Journal of the American College of Cardiology*, vol. 52, no. 6, pp. 446-449, 2008.

[1.17] P. L. M. J. van Neer, *Ultrasonic Superharmonic Imaging*, PhD thesis: Department of Biomedical Engineering, Erasmus University, 2010.

[1.18] J.N. Hilberath, D.A. Oakes, S.K. Shernan, B.E. Bulwer, M.N. D'Ambra, H.K. Eltzschig, "Safety of Transesophageal Echocardiography", http://www.asecho.org/files/JASE2010Nov.pdf, 2010.

[1.19] J. H. Lau, *Low Cost Flip Chip Technology for DCA, WLCSP, and PBGA Assemblies*, New York: McGraw-Hill, 2000.

# *Ultrasound Transducers*


Ultrasound transducers are devices that are capable of converting energy between the mechanical domain and the electrical domain. They are indispensable elements in ultrasound imaging systems. Before we dive into the system design, an in-depth understanding of ultrasound transducers is essential. Therefore, this chapter begins with a brief introduction to ultrasound transducers. Although there are different types of transducers, we will restrict ourselves to the study of piezoelectric transducers, which are the most widely used in medical ultrasound imaging. Afterwards, several important characteristics associated with ultrasound signals will be discussed, such as the reflection at tissue boundaries, the attenuation of the ultrasound wave during propagation, signal dynamic range, and harmonics generation. These are the foundations for ultrasound signal processing. The final part of this chapter is devoted to the analysis of the transducers that are used in this thesis work. As described in Chapter 1, the major tasks of this thesis work are to design an interface ASIC for the receive (Rx) transducer and to develop a technology for the transducer-to-chip interconnection. Therefore, in this chapter great emphasis is placed on the study of the Rx transducer. Based on the characteristics of this transducer, considerations on interconnection and electronics designs will be given.

## 2.1 A Short Introduction to Piezoelectric Ultrasound Transducers

### 2.1.1 Piezoelectric Effect

The fundamental working principle of a piezoelectric ultrasound transducer is based on the piezoelectric effect. When a mechanical force in the form of an ultrasound wave is applied to a transducer, along with geometric deformation, polarization of the electrical dipoles in the transducer dielectric occurs. Thus, a net dipole moment is created, which forms an electric field across the two electrodes of the transducer [2.1]. The polarization is proportional to the mechanical force, and changes sign depending on the sign of the pressure wave [2.2]. Inversely, if an ultrasound transducer is excited with alternating electric fields, it will compress and expand, and thereby generating sound waves in the ultrasonic range.

Many crystalline materials can be used to build piezoelectric ultrasound transducers, which can be categorized as natural crystals (e.g. quartz, Rochelle salt) or man-made ceramics (e.g. barium-titanate ceramics, lead-zirconate-titanate ceramics). Among them, the lead-zirconate-titanate ceramic, known as PZT, is the most widely used material [2.3]. It is also the building material for transducers used in this thesis project. It is worth noting that the piezoelectric property of a PZT ultrasound transducer will be lost if the temperature of the crystal rises above its Curie temperature. The temperature requirement puts constraints on the transducer-to-chip interconnection technology. Therefore, we should keep the processing temperature well below the Curie temperature of the selected PZT ceramic.

### 2.1.2 Device Structure

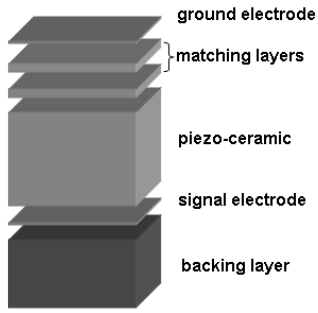



Fig. 2.1 Structure of a typical piezoelectric transducer (exploded view).

A typical piezoelectric ultrasound transducer is a layered device consisting of two electrodes, a piece of piezo-ceramic, a backing layer and one or more matching layers (Fig. 2.1). The electrodes should be sufficiently thin so that their influence on wave propagation is negligible [2.2]. The piezo-ceramic is the actual ultrasound generator and detector, which is sandwiched between the signal electrode and the ground electrode. The size and shape of the piezo-ceramic determine the resonance frequency of the transducer, at which the energy-conversion efficiency of the transducer reaches its highest value [2.4]. The frequency response of a piezoelectric ultrasound transducer has a band-pass shape. The bandwidth determines the range of frequencies over which the transducer can operate with relatively high energy conversion efficiency.

Since the acoustic impedances between the piezo-ceramic and the tissue being imaged differ greatly (e.g. the acoustic impedance of PZT ceramic is about 20-30 times higher than that of soft tissue [2.5]), connecting the piezo-ceramic directly to the tissue would cause strong reflection at the boundary. In this case, in the transmit mode, only a small percentage of the acoustic energy would then be transmitted into the tissue. The reflected waves would cause unwanted ringing of the piezo-ceramic, which would degrade the axial resolution (discussed in Section 2.1.5) of the image due to very long pulse

duration. Moreover, in the receive mode, large reflection would result in a low sensitivity.

To improve the energy transfer efficiency at the transduce-tissue boundary and enhance the sensitivity, one or more matching layers are employed. Matching layers have acoustic impedance levels between those of the piezo-ceramic and the tissue. The use of matching layers allows the sound waves to reflect back and forth repeatedly inside the matching layers, producing waves that are in phase to each other. Hence, waves are constructively added up to form a reinforced wave that propagates across the boundary. In this way, the sensitivity of the transducer is improved. In addition to the aforementioned advantage, as described in [2.5], by using several matching layers to gradually bridge the gap of acoustic impedances between the tissue and the piezo-ceramic, the bandwidth of the transducer can be tuned. In the meantime, to overcome the ringing problem, a backing layer (Fig. 2.1) is attached underneath the piezo-ceramic, so that during transmission, most of the energy reflected back into the piezo-ceramic can be absorbed and turned into heat. The backing layer also provides damping to the received echo signals. The durations of the echoes are as well shortened for better axial resolution.

### 2.1.3 Electrical Impedance Model

The electrical impedance looking into the two electrodes of a transducer can be modeled using a lumped-element model. Once the transducer design is completed, the electrical impedance model can be obtained by firstly measuring the device using an impedance analyzer and then applying curve fitting to find the values of the model parameters. Figure 2.2a shows a typical electrical impedance model. It consists of a series RCL resonance tank ($L_s$, $C_s$, $R_s$) and a shunting capacitor $C_p$. The series connection of $L_s$, $C_s$ and $R_s$ creates the so-called “motion branch”, which is devoted to the description of the mechanical part of the transducer [2.6]. The inductance $L_s$ represents the inertial effect of the piezoelectric material in vibration. The capacitance $C_s$ represents the elastic stiffness and $R_s$ relates to the energy

dissipation and mechanical loading. The shunting capacitor $C_p$ represents the dielectric property of the piezoelectric material.

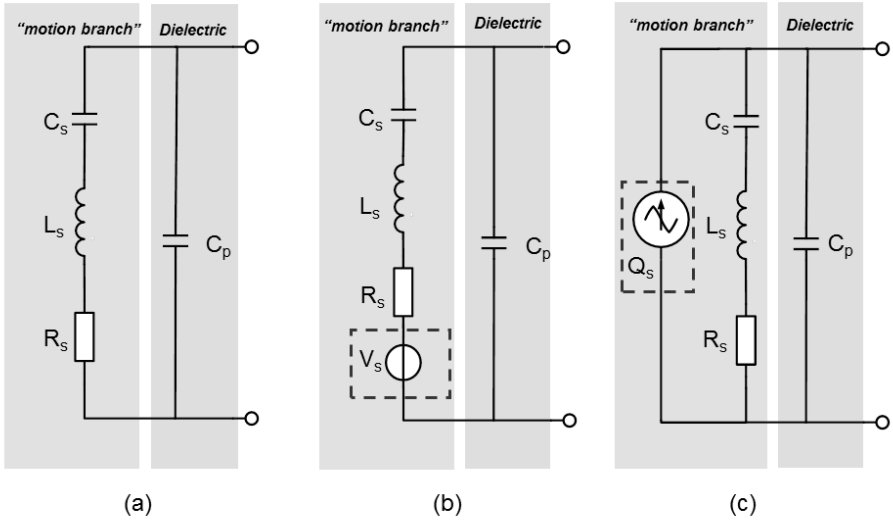



Fig. 2.2 Electrical model of a piezoelectric transducer: (a) typical impedance model, (b) electrical model in the receive mode (expanded model with a voltage source presented) and (c) electrical model in the receive mode (expanded model with a charge source presented).

The impedance model is useful for analyzing the transducer frequency response. Besides, during the front-end electronics design, the impedance model can be plugged into the circuit simulator for co-simulation. In the transmit mode, the transducer acts as a load. By including the impedance model into simulation, the required drive current, ring-down effects and power transfer can be calculated [2.7]. In the receive mode, the transducer acts as a sensor and senses dynamic mechanical excitations, i.e., changing forces. As indicated in [2.6], using an electromechanical analogy, the dynamic mechanical excitation is introduced in the form of a voltage source that is coupled to the "motion branch". To obtain an electrical model in the receive mode, the impedance model can be expanded to include a voltage source $V_s$ in series with the "motion branch" (Fig. 2.2b). This voltage source mimics the transduction between the mechanical domain and the electrical domain, which has a voltage directly proportional to the force and can have

an arbitrary frequency determined by the excitation source. The output voltage measured across the two output terminals of the transducer model can be understood as the voltage $V_s$ passes through a filter network [2.8]. It is worth noting that, using circuit theory, the voltage source shown in Fig. 2.2b can be transformed into a charge source (Fig. 2.2c), which represents the displacement of the piezoelectric transducer. The charge source model is convenient when displacement is a measurand and a charge amplifier can be used to interface the transducer. Moreover, one difference between the voltage source and the charge source is that the charge source is frequency-dependent.

### 2.1.4 Transducer Arrays and Beamforming

Most ultrasound transducers that are used for medical imaging are arrays. An array transducer is constructed with many transducer elements that arranged in a line, in a ring or in a 2D matrix pattern. By using a so-called "beamforming" technique [2.2], an array transducer allows the steering and focusing of ultrasound beams at various angles and at different depths, without physically moving the transducer. An array transducer also provides the flexibility to adjust the active aperture size to meet the requirements for lateral resolution and beam shape. The beamforming function is realized by a beamformer circuit, which determines the shape, size and position of the beams. An illustration is shown in Fig. 2.3. In the transmit mode, a transmit beamformer generates signals with relative delays to drive the individual transducer element in an array, so that beams can be steered to scan various angles and be focused at different depths (Fig. 2.3a). In the receive mode, a receive beamformer provides appropriate electrical delays to the echo signals received by the individual transducer elements and coherently sum them up to form a stronger electrical signal (Fig. 2.3b).

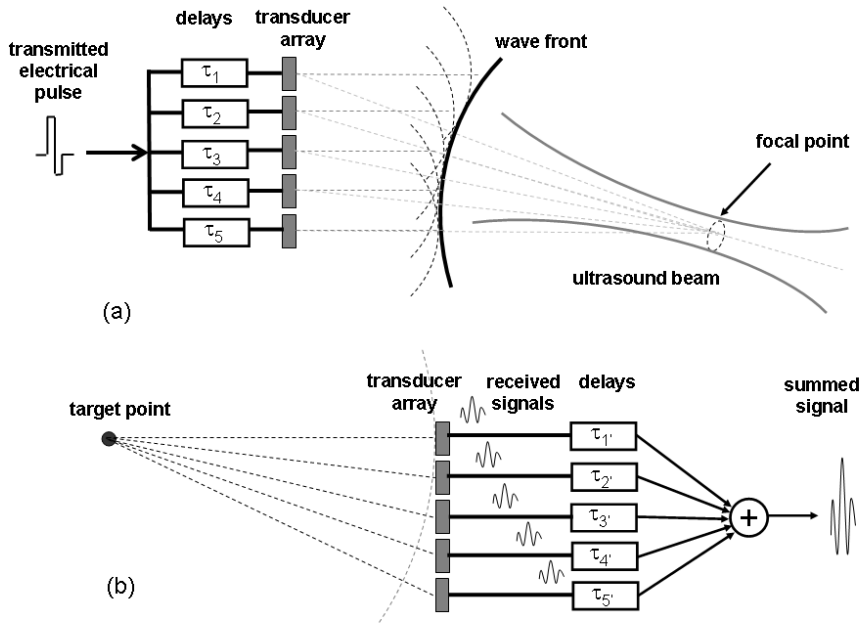



Fig. 2.3 Illustration of beamforming function: (a) transmit mode, (b) receive mode.

### 2.1.5 Transducer Resolution

Transducer resolution is defined as the smallest distance between two targets that can still be distinguished and displayed separately. It can be categorized into the axial resolution (parallel to the path of sound propagation) and the lateral resolution (perpendicular to the path of sound propagation).

Axial resolution is strongly dependent on the lengths of the transmitted acoustic pulses. An example is given in Fig. 2.4a. Assume the transmitted pulse has a length of *L* and points A, B, C and D are the objects along the axis of the ultrasound beam. Since the distance between two objects A and B is larger than *L*, they reflect pulses one after another. Therefore, they can be distinguished as two separate points. However, targets C and D have a distance smaller than *L*. The reflected pulses are no longer separate. It can be concluded from the above illustration that a shorter pulse length leads to a better axial resolution. To obtain a short pulse length, a well-designed transducer (matching layer at the front and backing layers) is required to

effectively dampen the vibration of the piezo-ceramic. Moreover, the shape of the electric excitation pulse will also affect the acoustic pulse length [2.9][2.10]. For a given transducer, the excitation pulse shape can be optimized to achieve the best axial resolution.

Lateral resolution refers to the ability to resolve two targets side by side perpendicular to the sound propagation direction. A narrower ultrasound beam width provides a better lateral resolution. Figure 2.4b shows an example. Assume the ultrasound beam at a certain axial depth has a width of $W$, and points E, F and G are targets perpendicular to the sound beam. Targets E and F are located within the beam width and they will appear as one point on the display. Target G is located separatelyt from targets E and F, thus, it can be displayed as a separate point. The beam width depends on the transducer aperture size, focal distance and wave length. A larger aperture size, higher frequency and a shorter focal length result in a narrower beam width and thus better lateral resolution [2.5].

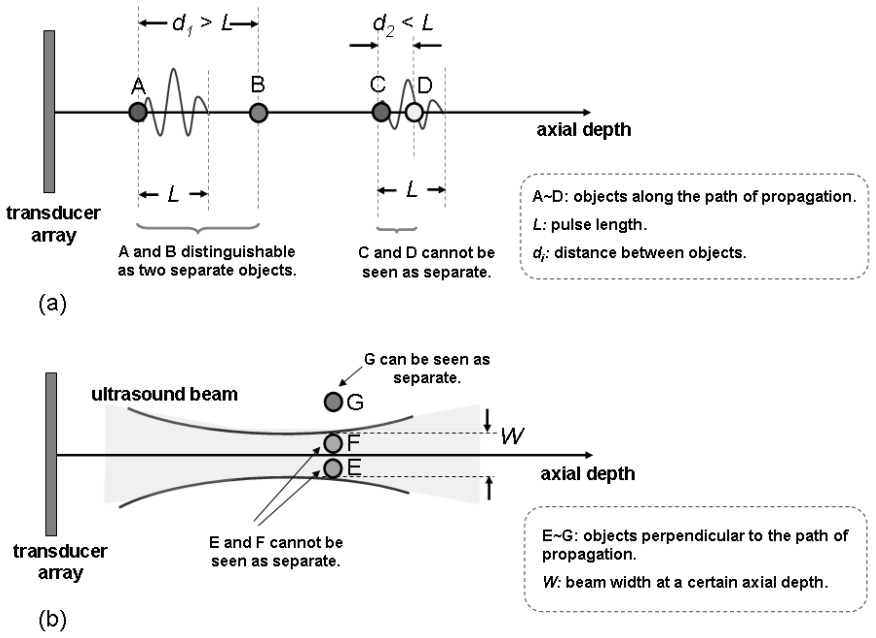



Fig. 2.4 Illustration of transducer resolution: (a) axial resolution, (b) lateral resolution.

## 2.2 Characteristics of Ultrasound Signals

### 2.2.1 Reflection and the Time-of-Flight (ToF) Principle

Conventional ultrasound imaging systems are based on the pulse-echo principle. As shown in Fig. 2.5, when ultrasound pulses generated by a transducer are propagating through inhomogeneous tissues, reflections occur at tissue boundaries due to differences in acoustic impedances. Then echo signals received by the transducer are sequences of reflected pulses over time. The axial depths that correspond to echoes can be calculated by tracking the time-of-flight (ToF). Since the values for the speed of sound in human soft tissues are rather similar, an average value of 1540 m/s can be used as the nominal value without introducing significant errors to the image [2.5]. Thus, once we know the arrival time of the reflected pulses, by multiplying the arrival time with the sound speed, the axial depths at which reflections occurred can be derived.

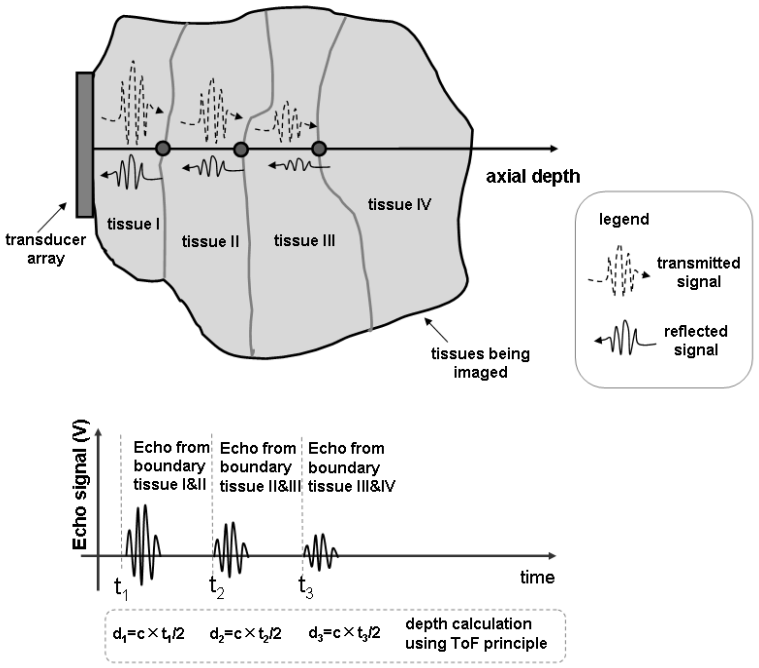



Fig. 2.5 Reflection phenomenon at tissue boundaries and the time-of-flight (ToF) principle.

### 2.2.2 Propagation Attenuation

When ultrasound waves are traveling in tissue, they experience energy loss. Two effects play a major role in this energy loss: absorption and scattering [2.2]. Absorption refers to the process whereby ultrasound energy is converted into heat. Scattering means the redirection of ultrasound waves. Those waves will deviate from the desired propagation path and will not be detected by the transducer. Comparing these two effects, absorption causes more attenuation than scattering [2.2].

A measure of energy loss along the ultrasound propagation path is the attenuation coefficient, which is expressed in dB/cm. For most tissues, the attenuation coefficient increases approximately linear with frequency [2.5]. Therefore, for ease of calculation, the attenuation is usually measured in dB/cm/MHz. For example, if a tissue attenuates by 0.5 dB/cm/MHz, then for a 5 MHz ultrasound signal that travels into the tissue, the attenuation at a

depth of 10 cm is approximately: (0.5 dB/cm/MHz) × 5 MHz × 10 cm = 25 dB.

### 2.2.3 Dynamic Range of the Received Signal

The electrical signal produced by an ultrasound transducer in the receive mode has a certain intrinsic dynamic range. The upper bound is mainly related to the transmit acoustic power. The larger the transmit power, the larger the received signal level. However, the transmit power cannot be arbitrarily high, but has to comply with the regulations set by the FDA (Food and Drug Administration, USA) [2.11] in order to avoid potential risks to the human body, such as tissue heating and cavitation. As for the lower bound, the electrical noise of the transducer itself sets the level of the minimum detectable signal. In reality, ultrasound transducers are used in imaging systems. The readout electronics in imaging systems inevitably have noise, which results in a reduced overall system dynamic range compared to the intrinsic dynamic range of the transducer. Therefore, the noise of the readout electronics must be minimized by careful design. For today's ultrasound machines, the maximum signal dynamic range is in the order of 120 dB [2.7].

Figure 2.6 illustrates the relationship of the received electrical signal level of an ultrasound transducer and the axial depth. It can be seen that the received signals are located in a belt called "instantaneous dynamic range", which can be understood as the received-signal dynamic range at each imaging depth. However, as discussed in Section 2.2.2, ultrasound signals experience propagation attenuation. The signal level reduces when the imaging depth increases, and finally is drowned out by the noise of the transducer (if we assume for now the noise of the readout electronics is negligible). The instantaneous dynamic range and the dynamic range due to propagation attenuation constitute the overall dynamic range of the received signal.

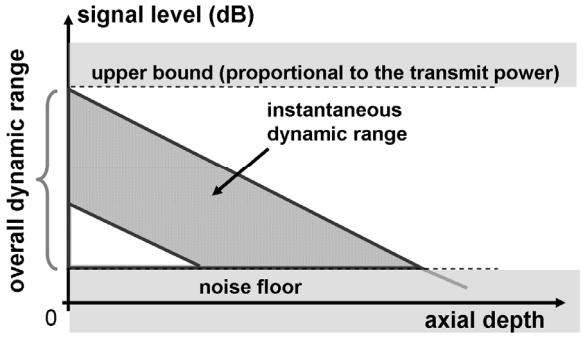



Fig. 2.6 Illustration of the signal dynamic range in the receive mode.

### 2.2.4 Signal Distortion and Harmonic Generation

The propagation of ultrasound waves in the tissue is non-linear, which results in the generation of harmonics. Take a simple sinusoidal wave as an example. Since the speed of sound is associated with pressure, the wave crests, which have higher pressure propagate faster than the wave troughs which have lower pressure. Gradually, distortion increases and the wave shape changes from a sine wave into a saw-tooth shape. A theoretical saw-tooth signal contains the fundamental frequency and an infinite number of harmonics.

Over the past decade, the non-linear property of ultrasound propagation opened up a new research direction called "ultrasound tissue harmonic imaging" [2.12]. Imaging techniques, such as "second-harmonic imaging" [2.13], and even "super-harmonic imaging" have been reported [2.14]. Compared to fundamental imaging, harmonic imaging has a number of advantages, e.g. enhancement of lateral and axial resolutions, a lower grating lobe level, and near-field artifact elimination.

In our project, we are investigating the feasibility of using the "second-harmonic imaging" technique for 3D TEE application. In the transmit mode, an ultrasound transducer transmits signals at the fundamental frequency, while second-harmonic components are generated during propagation due to inhomogeneity in media. In the receive mode, the reflection and scattering of

this second-harmonic signal is detected. To understand the properties of the second-harmonic waves, proper modeling of non-linear acoustic wave fields in inhomogeneous biomedical tissue is required. This topic has been investigated by team members Demi et al. [2.15][2.16]. There are challenges associated with the imaging system design when using the second-harmonic imaging technique. As reported in [2.15][2.16], second-harmonic signals are expected to be about 1~2 orders of magnitude lower than fundamental signals. Moreover, the second harmonic signals have doubled frequency compared to fundamental signals, thus they are attenuated more on their way back. In order to maintain a reasonable dynamic range for the received second-harmonic signal, sufficient transmit power is needed. However, as described in Chapter 1, for 3D TEE application the power dissipation in the probe tip is a critical design aspect, that also limits the transmit power. This issue is still under investigation.

## 2.3 Matrix Transducer for 3D TEE

### 2.3.1 Transducer Configuration for 3D TEE

As described in Chapter 1, in our design, we use two transducer sub-arrays to act separately as the transmitter and the receiver. The "second-harmonic imaging" technique is chosen and the designs of sub-arrays are optimized for the 3D second-harmonic TEE. The proposed configuration has a 4 × 32 Tx sub-array that transmits ultrasound pulses at around 3 MHz and a 45 × 45 Rx sub-array that receives echo signals at around 6 MHz. The bandwidth of interest in the receive mode is from 4.5 MHz to 7.5 MHz. The two sub-arrays are placed next to each other and encapsulated in the tip of a TEE probe (Fig. 2.7). The elements in the Tx sub-array are directly connected to the external imaging system with 128 micro-coaxial cables. For the Rx sub-array, micro-beamforming [2.17] will be applied by using an interface receive ASIC to reduce the channel count from 2025 to about 250. In this way, the total number of micro-coaxial cables inside the gastroscopic tube can be kept within 400.

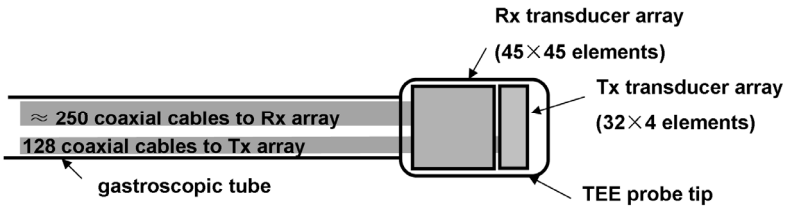



Fig. 2.7 Layout of the Tx and Rx transducers in a TEE probe.

During transmission, the rectangular shaped Tx sub-array transmits broad ultrasound beams to cover an elliptical volume. Later, parallel beamforming [2.18] is used in the receive mode, where the volume defined in the Tx mode is filled by a number of receive beams (see Fig. 2.8). It can be seen in Fig. 2.8a that close to the surfaces of two sub-arrays, there is insufficient overlap of the Tx beam and the Rx beam. As indicated in [2.18], with this design, from a depth of 30 mm, a large part of the transmit beam can be covered with receive beams.

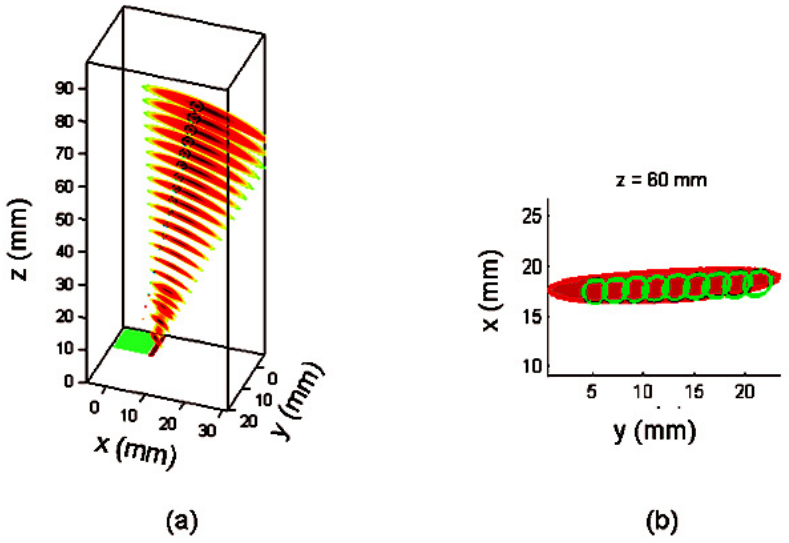



Fig. 2.8 Illustration of parallel beamforming [2.18] (courtesy of S. Blaak): (a) a broad transmit beam and a narrow receive beam, (b) the overlap between 9 parallel receive beams (circles) and a transmit beam (elliptic).

As described in Chapter 1, in this thesis, we focus on the electronics and interconnection designs for the Rx sub-array. Therefore, in the remainder of this section, we will focus on the Rx transducer, and the requirements for the electronics and interconnection scheme will be extracted.

### 2.3.2 Characteristics of the Rx Transducer

***Element geometry***

The optimal element geometry for the Rx sub-array has been investigated by team members van Neer et al., [2.4] using finite element methods (FEM). Each transducer element in the 45 × 45 array occupies an area of 0.17 mm × 0.17 mm. There is a 30 μm dicing kerf between adjacent elements. The total Rx sub-array measures 9.0 mm × 9.0 mm.

### *Material*

Piezo-material CTS 3203HD [2.19] was chosen to build the Rx (and Tx) transducer sub-array(s). This type of piezo-material has a Curie temperature of 225°C.

### *Electrical Model*

An Rx matrix transducer prototype has been manufactured by Oldelft Ultrasound B.V. The electrical impedance of 9 active transducer elements has been measured in water. Figure 2.9 shows the magnitude and phase diagrams for 9 elements. In order to acquire the parameters of the lumped-element impedance model for each measured element, we used ZView [2.20] for data fitting and model extraction. The extracted model is the same as shown in Fig. 2.2, and is redrawn in Fig. 2.10. It consists of a series RCL branch ($R_s$, $C_s$, $L_s$) that represents the mechanical part of the transducer and a shunting capacitor ($C_p$) that represent the dielectric property. Typical values for the model parameters are derived using data from the averaged magnitude and phase based on the measurement of 9 transducer elements. The fitting errors are also indicated in Fig. 2.10. Fig. 2.11 shows the modeled impedance plot (magnitude and phase) compared to the average impedance (magnitude and phase) obtained based on measurement.

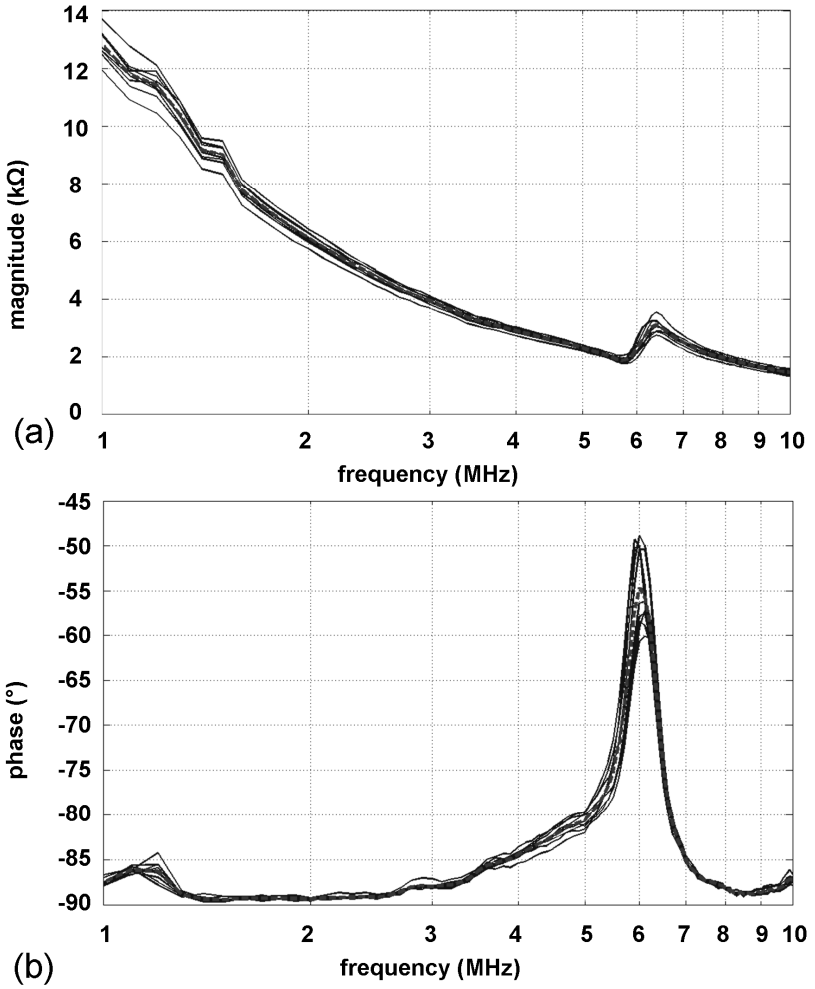
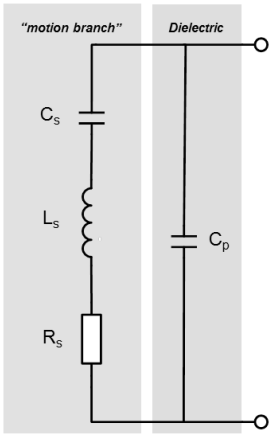



Fig. 2.9 Electrical impedance measurement of 9 Rx transducer elements: (a) magnitude plot, (b) phase plot. (dashed line: average value)




| Model parameters | Typical value* | Fitting error (%) |
|---|---|---|
| $R_s$ | 3.9 kΩ | 2.0 |
| $L_s$ | 0.64 mH | 2.0 |
| $C_s$ | 1.15 pF | 2.1 |
| $C_p$ | 11.27 pF | 0.27 |

* Typical value derived from the average impedance of 9 measured elements.

Fig. 2.10 Electrical model of the Rx transducer element with typical model parameters derived from the measured impedance of 9 transducer elements.

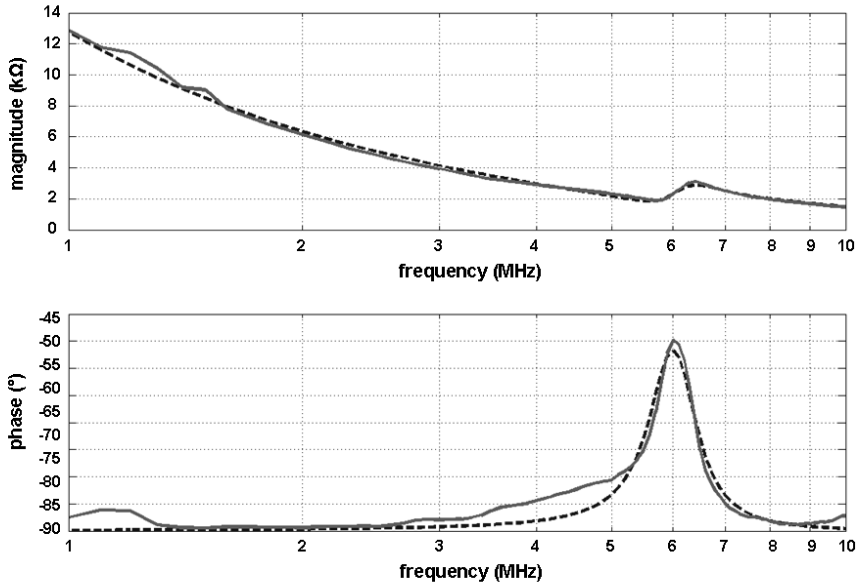



Fig. 2.11 Electrical impedance of the Rx transducer element: extracted model (dashed line) versus the average impedance (solid line) based on the measurement of 9 transducer elements.

For the interface receive electronics, the Rx transducer works as a signal source. As described in Section 2.1.3, a voltage source $V_s$ can be included in the impedance model (Fig. 2.12a). This voltage source mimics the transduction from the mechanical domain to the electrical domain and provides the signal that needs to be detected. The model in Fig. 2.12a can be transformed into a Thévenin equivalent circuit for easy observation of sensitivity variations among the elements. As shown in Fig. 2.12b, the equivalent circuit consists of two elements: the equivalent voltage source $V_{eq}$ and the equivalent source impedance. The equivalent source impedance is derived by shorting the voltage source $V_s$ and looking into the output terminals of the transducer. The resulting impedance is exactly the same as the impedance model shown in Fig. 2.11. It can be seen that at the resonant frequency, the average source impedance is about 2.5 kΩ.

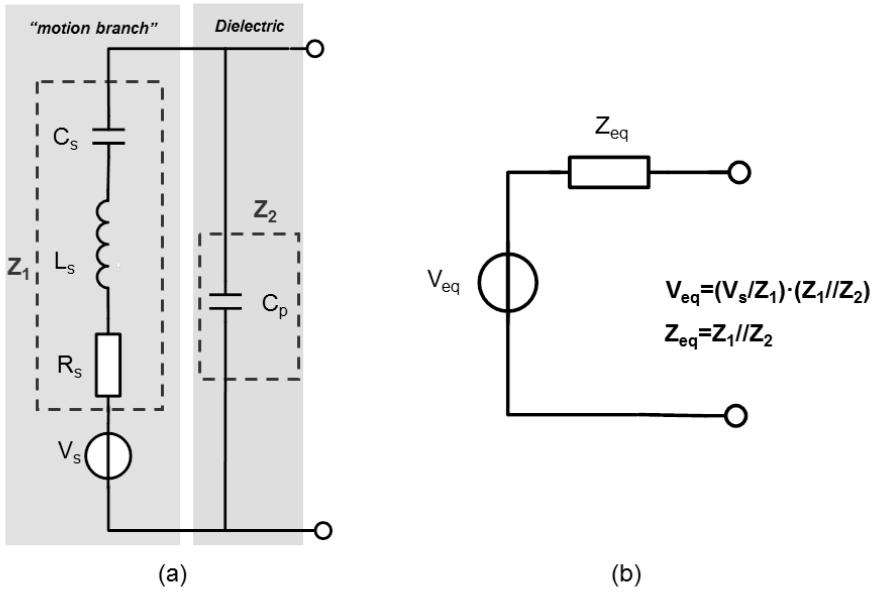



Fig. 2.12 Electrical model of a piezoelectric transducer element in the receive mode: (a) lumped model with a voltage source inserted in the "motion branch", (b) Thévenin equivalent circuit.

The equivalent voltage source $V_{eq}$ can be understood as the original source $V_s$ passing through a band-pass filtering network. Figure 2.13 plots the transfer function of the filtering network $H = V_{eq}/V_s$ using the typical model parameters. For our transducer, the frequency band of interest in the receive mode is from 4.5 MHz to 7.5 MHz, with a center frequency of 6 MHz. From Fig. 2.9, we can see that the transducer impedance varies from element to element. It is important to know how the impedance variations affect the sensitivities of transducer elements. The analysis on the transfer functions of the filtering network among various transducer elements gives us an order-of-magnitude estimation of the gain variations, or sensitivity variations, that are introduced by the transducer elements themselves. Figure 2.14 shows the transfer functions (gain plot) based on the model parameters of 9 elements. It can be seen from Fig. 2.14 that the sensitivity variation introduced by the transducer elements themselves is about 4 dB within the bandwidth of interest.

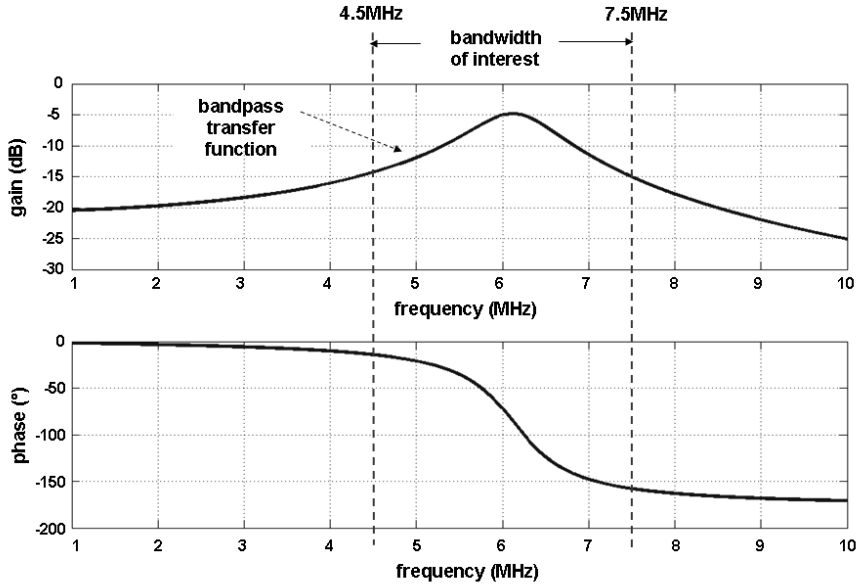



Fig. 2.13 Transfer function (gain plot) of the electrical filter network based on the transducer electrical model (typical model parameters are used).

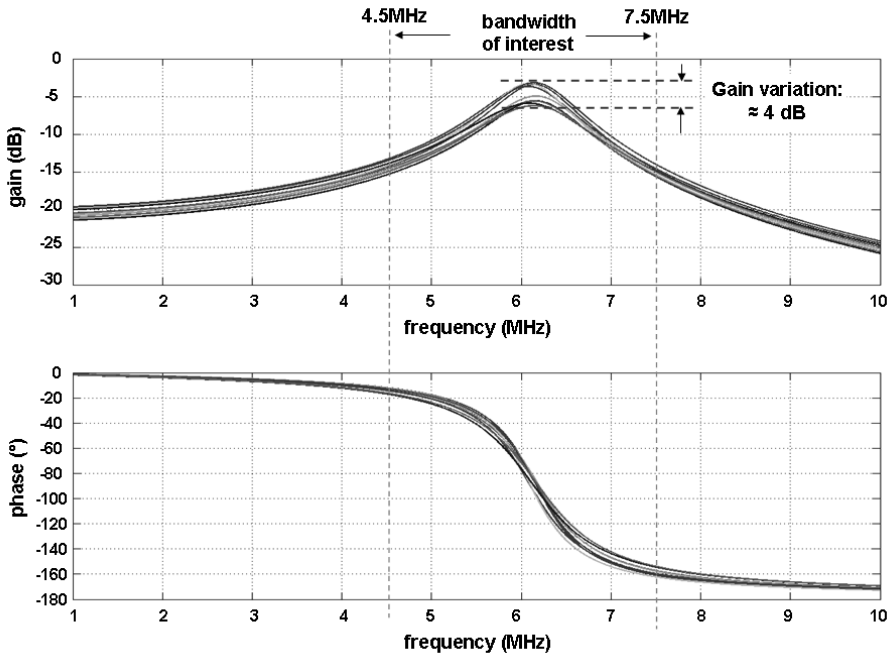



Fig. 2.14 Transfer function (gain plot) of the electrical filter network based on transducer electrical models (model parameters of 9 transducer elements are used).

### 2.3.3 Requirements for Interconnection and Rx Electronics

The analysis of the transducer characteristics provides important implications for the transducer-to-chip interconnection design and the Rx interface electronics design.

***For the transducer-to-chip interconnection design:***

- Geometric constraints

Since the space in the TEE probe tip is limited (length: 2 cm, width: 1 cm and height: 1 cm), the most space-saving assembly is to stack the ASIC and the Rx transducer. The overall structure including the Rx transducer, the ASIC, the intermediate layers for connection, plus the Tx transducer, must fit into the available space.

- Temperature constraints

The piezo-material used to build the Rx transducer (CTS 3203HD) has a Curie temperature of 225°C. To avoid de-polarization (see Section 2.1.1) of the piezo-material during the interconnection process, the process temperature must be controlled well below 225°C and preferably below 50% of the Curie temperature. This requirement imposes a restriction on the choices of interconnection solutions.

***For the Rx electronics design:***

- Area constraints

The area of the ASIC should fit within the area of the Rx transducer array. Slight extensions on three sides under the Rx transducer array are permitted. No extension is allowed on the fourth side of the ASIC, because this side is adjacent to the Tx transducer array (Fig. 2.6). The area directly underneath the Rx array is reserved for circuits and bond-pads arranged in a matrix pattern that can be connected to the Rx transducer array. The output signal pads, power pads and some control pads can be placed in the three extended side areas of the ASIC.

- Noise requirement for the readout electronics

As described in Section 2.2.3, the lower bound of the transducer detection limit is set by the noise of the transducer itself. The resistor $R_s$ in the impedance model (Fig. 2.10) is the noise source. It has a thermal noise density of about $6.75 \times 10^{-17}$ $V^2/Hz$ (calculated based on the typical model parameter $R_s = 3.95$ kΩ). The noise is band-pass filtered by the transducer impedance network. To have an order-of-magnitude estimation of the noise generated by the transducer element itself, we chose the bandwidth 4.5 MHz to 7.5 MHz as the noise bandwidth of the transducer. The resulting noise voltage is about 15 $\mu V_{rms}$ over the bandwidth of interest. In practice, the readout circuit will also introduce noise. A proper readout circuit should be designed in such a way that it should have an input referred noise level no larger than the noise level of the transducer element.

- Accuracy requirement

As analyzed in Section 2.3.2, the gain variation of the transducer elements is on the order of 4 dB. Elements with such gain variations are acceptable for producing ultrasound images with good quality. However, to ensure an overall accuracy of the ultrasound receiver, the gain variation of the receive electronics must be below the gain variations of transducer elements.

## 2.4 Conclusions

In this chapter, a comprehensive study on piezoelectric transducers is given. The contents cover the fundamental device physics of the transducers, their structure, the operating principle, their modeling, important signal characteristics, etc. Great emphasis is on the analysis of the Rx transducer, which has been chosen to be used for this thesis project. From the analysis, we obtained meaningful considerations for the electronics design, as well as the interconnection design, which will be presented in the following chapters.

## 2.5 References

[2.1] J. Karki, "Signal Conditioning Piezoelectric Sensors", *Texas Instrument Application Report*, SLOA033A, Sept. 2000.

[2.2] S.C. Cobbold, *Foundations of Biomedical Ultrasound*, Oxford University Press, 2007.

[2.3] A. Arnau, *Piezoelectric Transducers and Application*, Berlin: Springer, 2008.

[2.4] P.L.M.J. van Neer, *Ultrasonic Superharmonic Imaging*, PhD thesis: Department of Biomedical Engineering, Erasmus University, 2010.

[2.5] P. Hoskins, K. Martin, A. Thrush, *Diagnostic Ultrasound Physics and Equipment*, Cambridge University Press, 2010.

[2.6] MP Interconsulting, *Piezoelectric Transducers Modeling and Characterization*, Aug. 2004.
Available at: http://www.mpi-ultrasonics.com/transducers1.html

[2.7] K. Iniewski, *Medical Imaging, Principles, Detectors and Electronics*, New Jersey: John Wiley & Sons, 2009.

[2.8] http://en.wikipedia.org/wiki/Piezoelectric_sensor (July 2011).

[2.9] H.W. Persson, "Electric excitation of ultrasound transducers for short pulse generation", *Ultrasound in Med. & Biol*., vol. 7, pp.285-291, 1981.

[2.10] J. Salazar, A. Turó, J.A. Chávez, J.A. Ortega, M.J. García, "Transducer resolution enhancement by combining different excitation pulses", *Ultrasonics*, vol.38, pp.145-150, 2000.

[2.11] FDA Regulation, "Guidance for Industry and FDA Staff – Information for Manufacturers Seeking Marketing Clearance of Diagnostic Ultrasound Systems and Transducers", Sept. 2008. Available at: http://www.fda.gov/medicaldevices/deviceregulationandguidance/guidanceducments/ucm070856.htm#1 (January 2012).

[2.12] M.A. Averkiou, D.N. Roundhill, J.E. Powers, "A new imaging technique based on the nonlinear properties of tissues", *Proceedings IEEE Ultrasonics Symposium*, vol. 2, pp. 1561-1566, Toronto, Oct. 1997.

[2.13] F. Tranquart, N. Grenier, V. Eder, L. Pourcelot, "Clinical use of ultrasound tissue harmonic imaging", *Ultrasound Med Biol*. vol. 25, no. 6, pp. 889-94, Jul. 1999.

[2.14] P. L. M. J. van Neer, G. Matte, M.G. Danilouchkine, C. Prins, F. Van Den Adel, N. De Jong, "Super-harmonic imaging: development of an interleaved phased-array transducer", *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control*, vol. 57, issue 2, pp. 455-468, Feb. 2010.

[2.15] L. Demi, M. D. Verweij, N. de Jong, K. W. A. van Dongen, "Modeling nonlinear acoustic wave fields in media with inhomogeneity in the attenuation and in the nonlinearity", *Proceedings IEEE Ultrasonics Symposium*, 2010, pp. 2056-2059.

[2.16] L. Demi, M. D. Verweij, N. de Jong, K. W. A. van Dongen, "Modeling nonlinear medical ultrasound via a linearized contrast source method", *Proceedings IEEE Ultrasonics Symposium*, 2010, pp. 2175-2178.

[2.17] S. Blaak, Z. Yu, G.C.M. Meijer, C. Prins, C. T. Lancée, J. G. Bosch, N. de Jong, "Design of a micro-beamformer for a 2D piezoelectric ultrasound transducer", *Proceedings IEEE Ultrasonics Symposium*, 2009, pp. 1338-1341.

[2.18] S. Blaak, C. T. Lancée, J. G. Bosch, C. Prins, A. F. W. van der Steen, N. de Jong, "A matrix transducer for 3D transesophageal echocardiography with a separate transmit and receive subarray", *Proceedings IEEE Ultrasonics Symposium*, 2011.

[2.19] CTS Corporate, "PZT5A &5H Materials Technical Data", available at: http://www.ctscorp.com/components/pzt/downloads/PZT_5Aand5H.pdftransducer material. (January 2012).

[2.20] Scribner Associates, Inc., ZView, http://www.scribner.com/zplot-and-zview-for-windows-software-downloads.html (January 2012).

# *Front-End Receive-Signal Processing for 3D TEE*


In Chapter 2, the characteristics of an Rx ultrasound transducer that is optimized for 3D TEE imaging have been discussed. This transducer contains 45 × 45 elements and is located in the tip of a TEE probe. As introduced in Chapter 1, in order to make the signal acquisition of this transducer via a limited number (less than 250) of cables possible, a front-end application-specific integrated circuit (ASIC) is required to be bonded to the transducer and to provide "appropriate" signal processing in the probe tip to reduce the channel count. The meaning of the word "appropriate" is twofold. Firstly, the signal processing scheme must match with the signal characteristics of the transducer, so that useful information can be extracted from the output signals of the ASIC to form images. Secondly, since the ASIC is also located in the tip of the TEE probe, its size and power consumption cannot be arbitrarily large. Therefore, the signal-processing scheme must be designed in such a way that it is efficient enough to keep the ASIC compact and practically usable in a TEE probe. On the basis that the image quality is not degraded, simple signal-processing scheme is desired. With these considerations in mind, system-level studies have been carried out to derive an effective scheme for front-end signal-processing. The results are described in this chapter. Section 3.1 presents the proposed front-end

receiver-signal-processing chain, which consists of low-noise amplifiers (LNAs), time-gain-compensation (TGC) amplifiers and analog micro-beamformers. To reduce the design complexity, we made simplifications to the TGC scheme and the analog micro-beamforming scheme (Section 3.2). Section 3.3 gives an overview of the ASIC design and its associated requirements.

## 3.1 Architecture of the Receive-Signal Processing

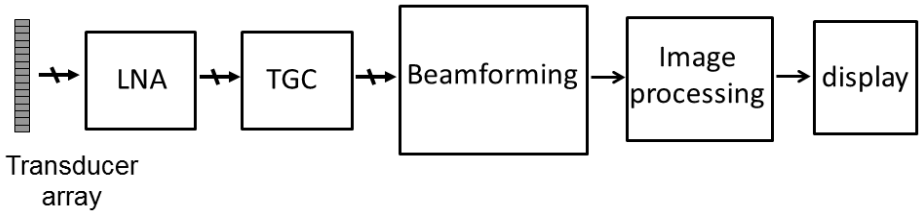



Fig. 3.1 Block diagram of a conventional receive-signal processing flow for ultrasound array transducers.

The block diagram of a conventional receive-signal processing flow for an ultrasound array-transducer is depicted in Fig. 3.1. It consists of five function modules: low-noise amplifiers (LNAs), time-gain-compensation (TGC) amplifiers, an Rx beamformer, an image processing module and a display module. Signals from transducer elements are first amplified by LNAs with a proper gain to boost the signal level above the noise level of the remaining circuitry. As described in Section 2.2.2, ultrasound signals experience propagation attenuation. Echo signals from deep tissue are more attenuated than those from nearby tissue and they also take more time to reach the probe. This time-dependent attenuation can be compensated for by using TGC amplifiers, which are able to amplify echo signals with a gain that increases exponentially with time (linearly in decibels). This compensation helps to maintain image uniformity and relaxes the dynamic-range requirements for the remaining circuitry. After TGC amplification, Rx

beamforming is applied. The beamforming principle is based on delaying the signals relative to each other in such a way that waves from a certain point, the focal point, arrive simultaneously and can be coherently summed. The summed signal is further processed in the imaging processing module, where envelope estimation, compression, etc., take place [3.1][3.2]. Finally, an image is formed which can be seen on the display.

In our 3D TEE application, the aforementioned Rx signal processing flow applies. However, for a practical implementation, proper partitioning of the system is necessary to divide the whole flow into a front-end and a back-end. The front-end processing is realized in an ASIC in the TEE probe tip, while the back-end processing occurs in an external imaging system.

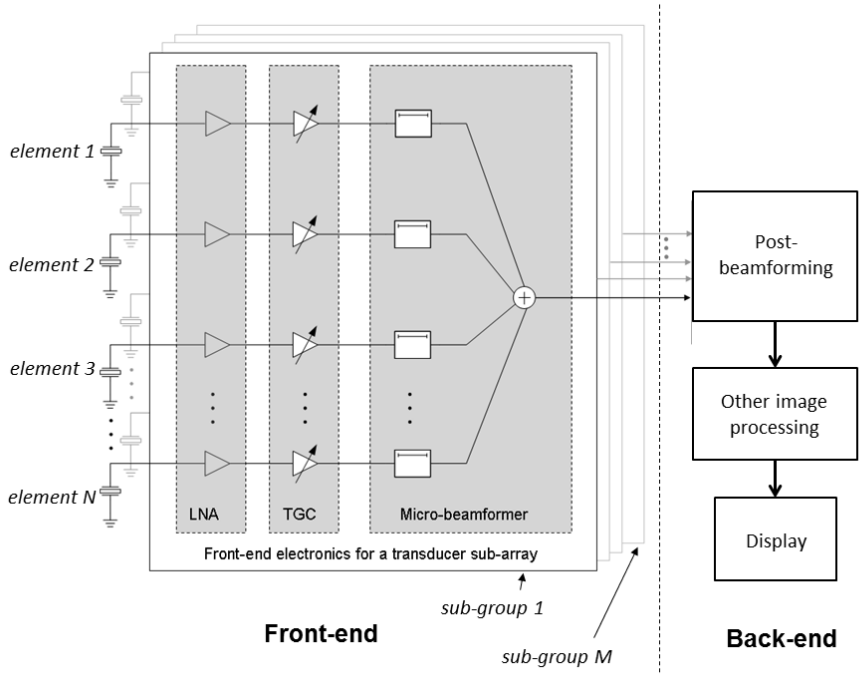



Fig. 3.2 Receive signal processing architecture for 3D TEE (N=9 and M=225).

As discussed above, in our project, an Rx transducer with 45 × 45 transducer elements is used and channel-count reduction in the probe tip is a must. Therefore, the delay-and-sum beamforming function is needed in the front-end processing. However, the complete beamforming function requires a

2025:1 channel count reduction, which is impractical to be fully implemented in the ASIC due to overcomplicated electronics. A greater channel-count reduction is likely to require more power consumption and more die area. In view of these factors, the so-called "sub-array beamforming architecture" [3.3] has been chosen. The complete beamforming task is divided into "pre-beamforming" or "micro-beamforming", which is implemented in the front-end ASIC, and "post-beamforming", which is implemented in the external imaging system. The micro-beamforming is done in such a way that the large matrix transducer is divided into sub-groups and delays are applied to signals received by the transducer elements within a group to align them in time (Fig. 3.2). Since elements in a sub-group are chosen to be close to each other in space, only fine delays are needed. Realizing these fine delays is feasible with front-end electronics in the TEE probe tip. The delayed signals are summed up to achieve the channel count reduction. We call the circuit which realizes the micro-beamforming function the "micro-beamformer". Each transducer sub-group has its own micro-beamformer. All micro-beamformers operate simultaneously and their output signals are transmitted via micro-coaxial cables to the external imaging system, where post-beamforming takes place. In post-beamforming, a coarse delay is applied to the signals from each sub-group, so that all the signals can be aligned in time and finally summed up.

To finalize the topology of the Rx signal processing chain, we still need to determine the size of the transducer sub-group. As discussed in Section 2.3.1, about 250 micro-coaxial cables are allowed in the gastroscopic tube for the Rx transducer. Since the power consumption and chip area in the TEE probe tip are critical factors, our design strategy is to provide just as much channel-count reduction as needed to make the system function properly with the number of cables available. To achieve the required channel count reduction from 2025 to about 250, each transducer sub-group should have more than 8 elements. In the mean time, to avoid too many delay steps and too long total delay time for transducer elements within a sub-group, the size of the sub-group should not be too large. To keep equal beamforming effects in the lateral and elevation directions, the size of the sub-group is chosen to be a square number ($3 \times 3$, $4 \times 4$, $5 \times 5$…, etc.). Besides, in our design, the "pre-

steering" technique is employed (see Section 3.2.2), acoustic simulations show that compared to a 4 × 4 or a 5 × 5 configuration, the 3 × 3 configuration produces a better acoustic field with a smaller grating lobe level. In Fig. 3.2, the front-end consists of 225 similar sub-blocks in parallel (M=225). Each sub-block interfaces 9 transducer elements (N=9) and contains 9 LNAs, 9 TGC amplifiers, and a micro-beamformer.

## 3.2 Simplifications in the Front-End Signal Processing Scheme

As discussed in the previous chapters, for the front-end ASIC in the TEE probe, several constraints apply, i.e., limited space, and a limited power budget. In view of this, simple, low-power electronics are preferred. Simplifications can be done hierarchically. We started with the "top-down" strategy. We first carried out investigations from the signal-processing perspective to find an efficient scheme that allows the use of simple electronics without degrading the image quality. Once the signal-processing scheme was fixed, further simplifications were made by properly selecting the circuit topologies. In this section, we present a simplified time-gain-compensation scheme and micro-beamforming method.

### 3.2.1 Time-Gain-Compensation Scheme

As discussed in Section 2.2.3, the dynamic range of the transducer output signal can be divided into two parts: the instantaneous dynamic range and the dynamic range due to propagation attenuation. In our 3D TEE application, the instantaneous dynamic range is ~40 dB. Combined with an estimated propagation attenuation up to 40 dB, this yields an overall signal dynamic range of 80 dB. The amplification by the LNAs enhances the signal levels and provides buffering for the transducers, which have high impedances. However, the dynamic range and the compositions of the signals at the inputs of the TGC amplifiers are unaltered (Fig. 3.3a). Ideally, the time-gain-compensation scheme should provide a gain that increases continuously with time in order to match the rate of propagation attenuation (Fig. 3.3b), so that after compensation only the instantaneous dynamic range

remains (Fig. 3.3c). This, however, requires either very fine discrete gain steps or an intricate continuous gain control, which complicates the design of the amplifier and would give rise to increased power consumption. Instead, a simpler implementation that provides only four discrete gain settings to cover a 40 dB gain range has been chosen (Fig. 3.3d) [3.4]. With this configuration, two control bits are required to set the gain. The timing of the gain switching is determined by an external control signal, and the active period for each gain setting is not necessarily equal. Figure 3.3d shows a 4-step compensation scheme with uniform gain-switching timing and uniform gain-step size (10 dB) for illustration purposes. As can be seen from Fig. 3.3e, after the compensation, the propagation attenuation is partially compensated for, thus significantly reducing the output dynamic range and relaxing the input dynamic range requirement of the micro-beamforming circuits. However, it can also be observed from Fig. 3.3e that the uniform gain-switching timing is not the optimal configuration, since the four parts of the instantaneous dynamic range are not perfectly aligned, which results in a remaining dynamic range that is slightly larger than strictly necessary. Moreover, in reality, the signal attenuation is non-linear. Therefore, we need to properly control the timing of the gain switching in order to achieve the optimal time-gain compensation.

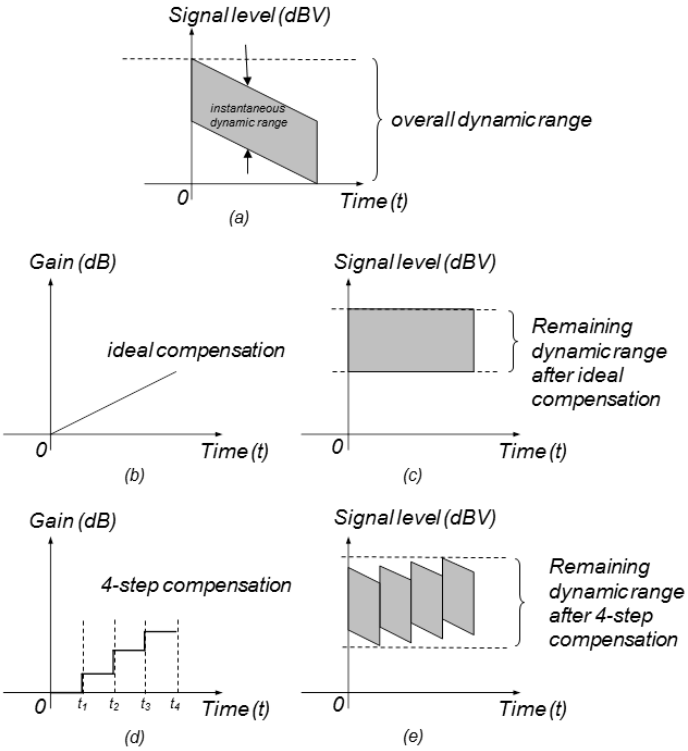



Fig. 3.3 Dynamic range of the ultrasound receiver system: (a) dynamic range at the input of the TGC amplifiers, (b) ideal TGC scheme, (c) output dynamic range after ideal TGC, (d) four-step TGC scheme, and (e) output dynamic range after four-step compensation.

## 3.2.2 Micro-Beamforming Scheme

### 3.2.2.1 Principle

As described in Section 3.1, the Rx transducer array is divided into 225 sub-groups. Each sub-group contains 3 × 3 elements. During micro-beamforming, fine delays are applied to the elements of each sub-group. In the ideal case, every transducer element should have its own specific fine delay. This corresponds to 225 groups of different delay settings. To implement these delay settings on-chip, 225 delay-control circuits are needed, which would be rather complex to realize. Instead of the ideal case, we proposed a simplified "micro-beamforming" scheme, in which all transducer sub-groups

are given the same fine delay pattern (Fig. 3.4). We call this implementation "pre-steering" [3.5]. Pre-steering effectively changes the neutral beam direction of the array by tilting all the groups to a certain angle. Although it introduces a small delay error with respect to ideal element-wise beam steering, the advantage is that the electronics can be kept simple, because all transducer sub-groups can share one delay configuration, instead of 225 different delay configurations. To reduce the complexity of the electronics even further, the required fine delay times are approximated by a set of fixed delay steps (i.e., a delay time per delay stage).

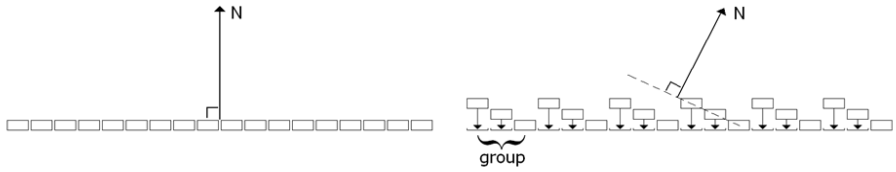



Fig. 3.4 Pre-steering changes the neutral direction N of the beam. The fine delays are indicated with the small arrows. All groups are given the same fine delay pattern.

### 3.2.2.2 Performance Evaluation by Acoustic Simulation

To predict the performance of the proposed micro-beamforming scheme, acoustic simulations have been carried out in the ultrasound simulation program Field II [3.5][3.6][3.7]. One of the major concerns when we divide transducer elements into groups is the grating-lobe level. Grating lobes appear when the field is spatially under-sampled. For example, when these elements would be grouped without micro-beamforming, each group would act as one large element. The spatial sampling interval (i.e., the pitch of the element) is larger than the ideal case, where each element can be addressed separately. Thus grating lobes are much more pronounced. Since, in our application, the instantaneous dynamic range of the echoes that are expected to return from the heart is about 40 dB, the level of the grating lobes should be more than 40 dB below the main lobe level to avoid imaging artifacts. In the proposed design, the transmit and the receive fields are separated (see Section 2.3.1). Since both contribute to reduce the grating-lobe level, for the

grating-lobe level in the received field an upper limit is set at -20 dB below the main lobe level.

In a first simulation, we investigated whether the pre-steering scheme can fulfill the requirement to keep the grating-lobe level below -20 dB. We considered a receive matrix transducer consisting of 45 × 45 elements, arranged in groups of 3 × 3, with an element pitch of 200 µm. The elements were excited with a Gaussian-shaped pulse with a center frequency at 6 MHz and a 50% bandwidth.

The receive-field was calculated on the surface of a hemisphere with a 60 mm radius and projected in the *x*-*y* plane (Fig. 3.5). The receive-beam patterns were calculated for varying elevation angles $\varphi$ and azimuth angles $\theta$. Three cases have been simulated:

- Case I: all elements were addressed separately and their ideal delays were applied.
- Case II: no pre-steering was applied. Elements were grouped (3 × 3) and the same coarse delay was applied to all group elements.
- Case III: the pre-steered case, where the elements were grouped (3 × 3), a coarse delay was applied to all group elements, and a separate fine delay was applied to each element of a group. The fine-delay patterns were identical for all groups.

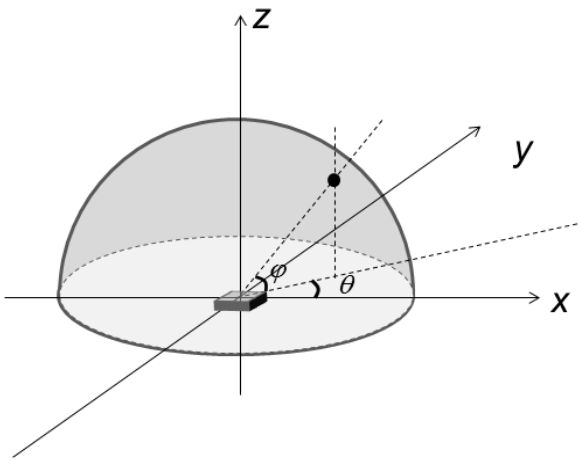



Fig. 3.5 The surface on which the beam patterns were calculated. The matrix transducer is located in the *x*-*y* plane with its center at the origin of the coordinate system. The elevation angle $\varphi$ is the angle between the axis of the beam and the *x*-*y* plane. The azimuth angle $\theta$ is the angle between the projection of the beam on the *x*-*y* plane and the *x*-axis.

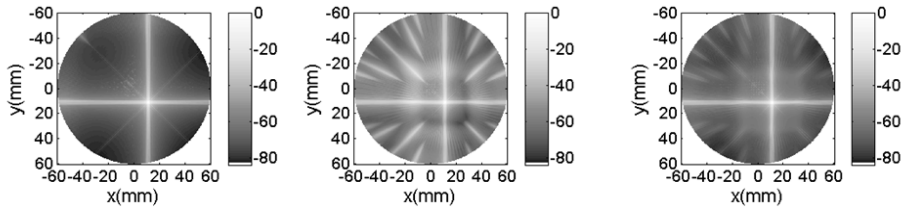



Fig. 3.6 The received pressure field for a matrix transducer with focus at 60 mm, a 75º elevation and a 45º azimuth: (a) when all elements have their own specific delays, (b) when the coarse delays are applied to the groups, and (c) when pre-steering is applied. The differences in the grating-lobe levels in cases (a) and (b) are clearly visible. In case (c), the grating lobes are significantly reduced.

Figure 3.6 shows the resulting beam patterns for the three cases in which the beam was focused at 60 mm and steered to a 75° elevation and a 45° azimuth. The maximum grating lobe levels for varying steering angles are

listed in Table 3.1. It can be seen that the pre-steering approach significantly reduces the grating lobe level, compared to the case in which no pre-steering is applied.

TABLE 3.1 MAXIMUM GRATING LOBE LEVEL FOR VARIOUS ELEVATION ANGLES $\varphi$ AND AZIMUTH ANGLES $\theta$.

| **Steering angle** | | **Maximum Grating lobe level (dB)** | | |
|---|---|---|---|---|
| **φ (°)** | **θ (°)** | **Case I** | **Case II** | **Case III** |
| 75 | 0 | -32 | -12 | -29 |
| 75 | 15 | -33 | -13 | -29 |
| 75 | 30 | -33 | -14 | -29 |
| 75 | 45 | -33 | -17 | -29 |
| 65 | 0 | -30 | 0 | -30 |
| 65 | 15 | -30 | -1 | -29 |
| 65 | 30 | -31 | -4 | -29 |
| 65 | 45 | -32 | -4 | -29 |
| 55 | 0 | -27 | -3 | -27 |
| 55 | 15 | -27 | -2 | -27 |
| 55 | 30 | -28 | 5 | -28 |
| 55 | 45 | -30 | 8 | -29 |
| 45 | 0 | -25 | -5 | -25 |
| 45 | 15 | -25 | -5 | -25 |
| 45 | 30 | -27 | 8 | -26 |
| 45 | 45 | -28 | 9 | -28 |

Next, simulations have been performed to determine the optimal delay step per delay stage. Beam patterns of the received field have been calculated for varying delay steps and the grating lobe level has been determined. The results are listed in Table 3.2. From this table it can be concluded that a delay step size of 40 ns will fulfill the requirement of a grating lobe level that is 20 dB below the main lobe level.

More detailed descriptions of the acoustic simulation can be found in Appendix A.

TABLE 3.2 THE MAXIMUM GRATING LOBE LEVEL FOR VARIOUS DELAY TIMES PER DELAY STEP. LEVELS THAT DO NOT MEET THE 20 DB CRITERION ARE PRINTED IN BOLD.

| **Steering angle** | | **Maximum Grating lobe level (dB)** | | |
|---|---|---|---|---|
| **φ (°)** | **θ (°)** | **40 ns** | **60 ns** | **80 ns** |
| 75 | 0 | -30 | -24 | **-19** |
| 75 | 15 | -25 | -24 | -21 |
| 75 | 30 | -26 | -27 | -21 |
| 75 | 45 | -27 | -26 | **-18** |
| 65 | 0 | -24 | -29 | -21 |
| 65 | 15 | -26 | -22 | -26 |
| 65 | 30 | -28 | -23 | -22 |
| 65 | 45 | -29 | -26 | -25 |
| 55 | 0 | -27 | **-18** | -27 |
| 55 | 15 | -27 | -23 | **-19** |
| 55 | 30 | -25 | -28 | -20 |
| 55 | 45 | -25 | -30 | -23 |
| 45 | 0 | -23 | -22 | -21 |
| 45 | 15 | -25 | -24 | **-19** |
| 45 | 30 | -25 | -24 | -22 |
| 45 | 45 | -27 | -25 | -26 |

### 3.2.2.3 Requirements for Delay Ranges

In Section 3.2.2.2, we concluded that the optimal delay step size in the micro-beamforming scheme is 40 ns. To have a better estimation of the circuit scale and the control logic complexity, we need to know the requirement on the programmable delay range for each transducer element in a 3 × 3 sub-group.

For each transducer sub-group with 3 × 3 elements, micro-beamforming directions in a cone with a 90° opening angle are considered (Fig. 3.7a). To simplify the delay calculation, we divided the cone into 8 sectors (Fig. 3.7b). As soon as the delay configurations to cover scan directions in one sector are known, because of the symmetrical geometry, the complete delay configurations to cover the whole cone could be determined.

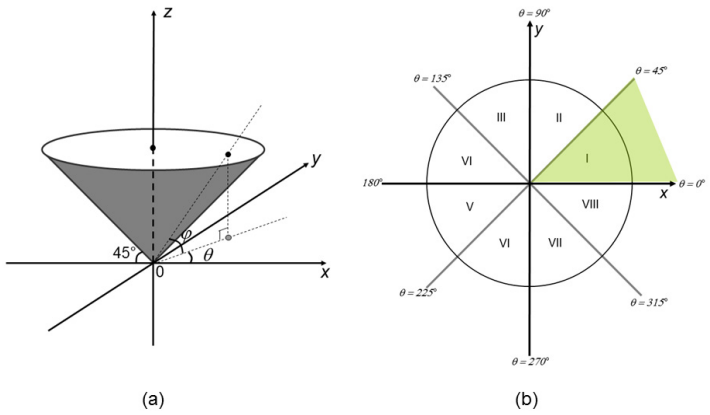



Fig. 3.7 Micro-beamforming directions: (a) micro-beamforming directions in a cone with a 90º opening angle are considered, and (b) view of the cone projected onto the *x*-*y* plane which is divided into 8 sectors.

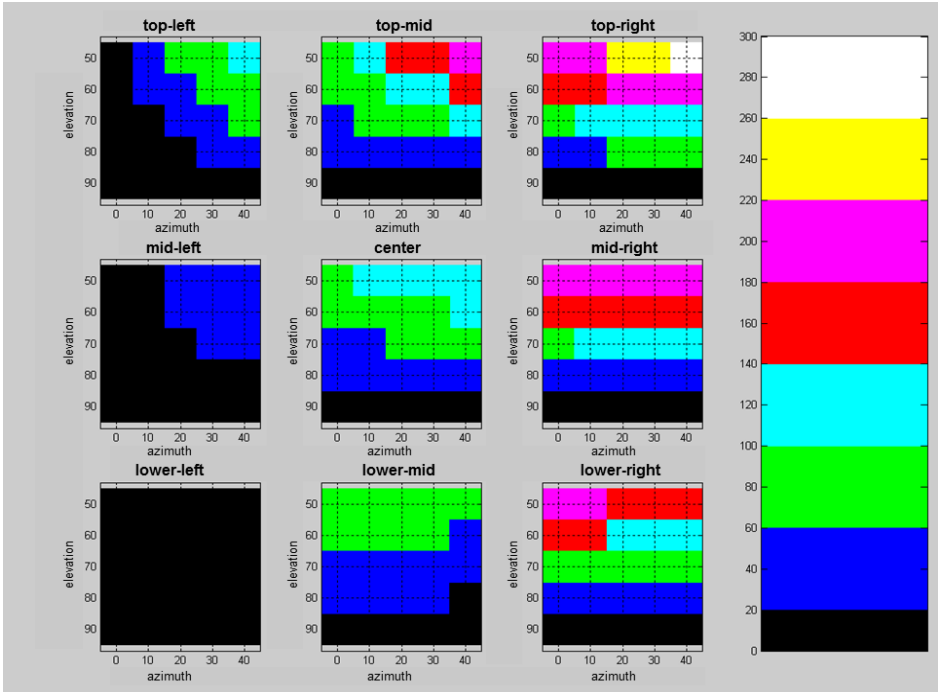



Fig. 3.8 Delay color map for the 3 × 3 elements in a transducer sub-group to cover the scan directions in sector I with a delay step size of 40 ns (courtesy of Dr. Charles Lancée).

Next, we calculated the delay configurations in sector I, which covers the elevation angles from 45° to 90° and azimuth angles from 0° to 45°. Figure 3.8 shows a delay color map which indicates the delay pattern for all the scan directions in sector I with a delay step size of 40 ns. The largest required fine delay is 280 ns, which occurs only once for the element in the upper-left corner at steering directions close to (elevation, azimuth) = (50°, 40°).

To derive the delay requirements for the transducer elements in a 3 × 3 sub-group to cover all the scan directions, we divided the elements into three categories (Fig. 3.9a): 1 center element, 4 side-middle elements (top-mid, mid-left, mid-right and lower-mid) and 4 corner elements (top-left, top-right, lower-left and lower-right). From Fig. 3.8 we have observed that to cover the scan directions in sector I the center element requires a delay range of 0 ns to 120 ns. The top-right-corner element requires a worst case delay range of 0 ns to 280 ns. The top-middle and mid-right elements have a worst case delay range of 0 ns to 200 ns. Based on the above analysis, while considering the symmetry of the transducer sub-array, we concluded that to cover all the scan directions for the center element, we need 4 programmable delay values (0, 40, 80, or 120 ns). The 4 side-middle elements and the 4 corner elements require programmable delays of 0 ns to 200 ns and 280 ns, respectively (Fig. 3.9b).

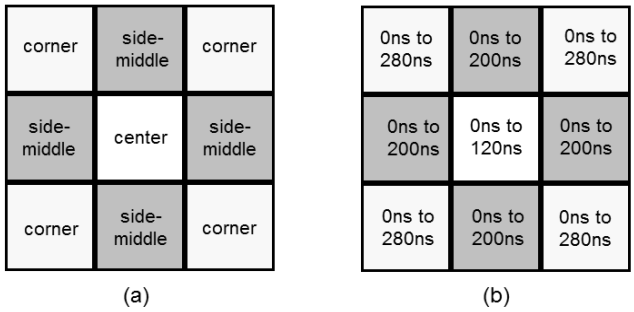



Fig. 3.9 Categorization and delay requirements for 3 × 3 elements in a transducer sub-group: (a) 9 transducer elements can be divided into 3 categories: 1 center element, 4 side-middle elements and 4 corner elements, and (b) required programmable delay ranges for elements in these 3 categories.

## 3.3 Front-End Receive ASIC Design Overview

The front-end receive ASIC consists of 225 similar sub-circuits in parallel. Each sub-circuit contains 9 LNAs, 9 TGC amplifiers and a micro-beamformer (Fig. 3.2). Signals from the transducer elements are firstly amplified by LNAs with a fixed gain to enhance the signal level above the noise floor of the remaining circuitry. As an initial estimation based on the input signal level, dynamic range and the power consumption consideration[1], we set the gain of the LNA to be 20 dB. Afterwards, TGC amplifiers with 4-step gains are applied to compensate for the propagation attenuation to cover the 40 dB gain range. Essentially, the TGC amplifier is a programmable-gain amplifier. Functionally speaking, the LNA can be treated as an additional gain stage of the TGC amplifier. A co-design of the LNA and the TGC amplifier is needed to obtain the most power-efficient solution, which will be presented in Chapter 4. Finally, micro-beamforming is applied by the micro-beamformer to align 9 output signals from the TGC amplifiers in time

[1] Power consumption consideration: There is a trade-off between the LNA gain and the power consumption. A higher gain implies more relaxed noise requirements for the TGC amplifier, so the TGC amplifier can consume less power. However, a high gain of the LNA requires more gain-bandwidth product (GBW) of the LNA itself, which leads to a larger power consumption.

and add them constructively. In addition to the general functionality described above, the ASIC should also fulfill the following design requirements:

- The total power budget of the ASIC is set to be on the order of 1W to 2W, but preferably not more than 1 W (Chapter 1).
- The ASIC must be able to handle input voltage signals in the bandwidth from 4.5 MHz to 7.5 MHz, with the center frequency of 6 MHz (Chapter 2).
- The ASIC must be able to interface single-ended input voltage signals (rms values) with an approximately 80 dB input dynamic range (15 μV~100 mV) (Chapter 2).
- As analyzed in Chapter 2, the noise voltage of the transducer elements is in the order of 15 $\mu V_{rms}$ in the bandwidth of interest (4.5 MHz ~ 7.5 MHz). The noise contribution of the ASIC must not be the dominant source.
- The gain variation of the transducer elements are in the order of ±2 dB (Chapter 2). The channel-to-channel gain variations of the ASIC must be small enough to be non-dominant.
- The ASIC must fit in the TEE probe tip.

## 3.4 Conclusions

In this chapter, a system-level study has been carried out to derive a proper front-end receive signal processing scheme for 3D TEE application. The proposed TGC scheme with four discrete gain settings, together with the proposed micro-beamforming scheme using pre-steering and discrete delay steps, greatly reduce the complexity of the circuit design. Acoustic simulations have been carried out to verify the effectiveness of the pre-steering method and to determine the required delay step size. Afterwards, delay ranges for various elements in a sub-group have been calculated. The proposed front-end signal processing scheme will be implemented in an ASIC. The function description and design requirements of the ASIC have also been given. The design choices for the function blocks of the ASIC are summarized in Table 3.3.

TABLE 3.3 DESIGN CHOICES FOR THE FRONT-END RECEIVE ASIC IN THE SIGNAL PROCESSING PERSPECTIVE.

| Function Block | Design Choice |
|---|---|
| LNA | • 20dB fixed gain<br>• 1 LNA per transducer element |
| TGC amplifier | • 4 discrete gains to cover 40dB gain ranges<br>• 1 TGC amplifier per transducer element |
| Micro-beamformer | • 1 micro-beamformer per 9 transducer elements<br>• Pre-steering is applied<br>• Delay step size: 40ns<br>• Required programmable delay ranges for 3×3 elements in a transducer sub-group:<br>o Center element: 0 ns to 120 ns<br>o Side-middle elements: 0 ns to 200 ns<br>o Corner elements: 0 ns to 280 ns |

## 3.5 References

[3.1] J. A. Jensen, *Estimation of Blood Velocities Using Ultrasound A Signal Processing Approach*, Cambridge University Press, 1996.

[3.2] R.S.C. Cobbold, *Foundations of Biomedical Ultrasound*, Oxford University Press, 2007.

[3.3] B. Savord, R. Solomon, "Fully sampled matrix transducer for real time 3D ultrasonic imaging", *Proceedings IEEE Ultrasonics Symposium,* 2003, pp. 945-953.

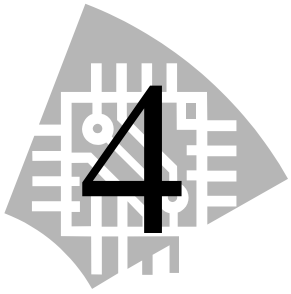
[3.4] J. Yao, Z. Yu, M. A. P. Pertijs, G. C. M. Meijer, C. T. Lancée, J. G. Bosch, N. de Jong, "Design of a low power time-gain-compensation amplifier for a 2D piezoelectric ultrasound transducer", *Proceedings IEEE Ultrasonics Symposium*, 2010, pp. 841-844.

[3.5] S. Blaak, Z. Yu, G. C. M. Meijer, C. Prins, C. T. Lancée, J. G. Bosch, N. de Jong, "Design of a micro-beamformer for a 2D piezoelectric ultrasound transducer", *Proceedings IEEE Ultrasonics Symposium*, 2009, pp. 1338-1341.

[3.6] J. A. Jensen, "Field: A program for simulating ultrasound systems", *Medical & Biological Engineering & Computing,* vol. 34, supplement 1, part 1, pp. 351-353, 1996.

[3.7] J. A. Jensen, N. B. Svendsen, "Calculation of pressure fields from arbitrarily shaped, apodized, and excited ultrasound transducers", *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control,* vol. 39, issue. 2, pp. 262-267, 1992.

# *LNA and TGC Amplifier Designs*




In Chapter 3, a front-end signal processing architecture for 3D TEE has been discussed. The complete front-end ASIC consists of three function blocks: low-noise amplifiers (LNAs), time-gain-compensation (TGC) amplifiers, and micro-beamformers. This chapter describes the designs of the LNA and the TGC amplifier. The key requirements and choices made for the LNA and TGC amplifier designs are presented in Section 4.1. This is followed by the circuit implementations of the LNA and the TGC amplifier in Section 4.2 and Section 4.3, respectively. Finally, we conclude this chapter in Section 4.4.

## 4.1 Design Requirements and Choices

As discussed in Chapter 3, with the simplified TGC scheme, the TGC amplifier has essentially been turned into a programmable-gain amplifier which is capable of providing 4-step gains to cover a 40 dB gain range. Meanwhile, the LNA provides a fixed-gain of 20 dB. Functionally speaking, the LNA can be treated as an additional gain stage of the TGC amplifier. The design target is to obtain a low-power solution for the combined LNA-TGC amplifier.

## *Design Requirements*

For the combined LNA-TGC amplifier, several requirements apply:

- The combined LNA-TGC amplifier requires an input that is matched to the ultrasound transducer in terms of impedance, noise level, bandwidth, etc. As discussed in Chapter 2, the signal source, i.e., the Rx transducer, has a single-ended nature. It can be modeled as a voltage source with a source impedance of about 2.5 kΩ. The output noise voltage of the signal source is in the order of 15 $\mu V_{rms}$ in the bandwidth of interest (4.5 MHz ~ 7.5 MHz). Therefore, the input-referred noise of the combined LNA-TGC amplifier must be equivalent to or lower than the noise of the transducer.
- The combined LNA-TGC amplifier requires an output that is matched to the micro-beamformer. The micro-beamformer, which will be presented in Chapter 5, is a differential circuit. Therefore, a single-ended-to-differential conversion is required for the combined LNA-TGC amplifier. Moreover, the output stage of the circuit must be capable of driving 250 fF capacitive loads, which are the input capacitances of the micro-beamformer for both positive and negative rails in the differential output port.
- The gain variation of the combined LNA-TGC amplifier among the channels must be well below the sensitivity variation of the transducer elements, which is about ±2 dB based on the measurement results shown in Chapter 2 on 9 transducer elements.
- The targeted power budget for a combined LNA-TGC amplifier is 250 μW. If we scale this number up for 45 × 45 input channels, the total targeted power consumption is about 500 mW.

## *Design Choices*

- Since the LNA can be treated as an additional gain stage of the TGC amplifier, one approach of the LNA-TGC co-design is to apply an overall feedback topology and simply design the TGC amplifier with an initial gain of 20 dB. In other words, the LNA can be eliminated.

However, if we would do so, we need a rather large gain-bandwidth product (GBW) while maintaining the required noise level, which would lead to large power consumption. Instead, we have chosen to stick to the multi-stage topology, i.e., an LNA and a TGC amplifier in cascade.

- The LNA is required to have the lowest input-referred noise. It is likely the most power-hungry stage. To obtain a power-efficient implementation, we have chosen to use a simple open-loop single-ended topology. The task of the single-ended-to-differential conversion is chosen to be implemented in the TGC amplifier.
- The simple open-loop topology of the LNA comes at the cost of large gain errors. Since the LNA and the TGC amplifier are in cascade, the gain errors of the two circuit blocks add up. In order to ensure reasonable overall gain accuracy, we have chosen to allocate the majority of the gain-error budget to the LNA. Meanwhile, we have chosen to use a closed-loop approach in the TGC amplifier in order to obtain a low enough gain-error contribution.
- Another limitation of a simple open-loop LNA is its poor linearity. One concern is the harmonic distortion due to the non-linear amplification [4.1]. In Section 2.3.1, we described that in our project the second-harmonic imaging technique has been chosen. The transmitted ultrasound pulses have a center frequency of 3 MHz, and a receive (Rx) array receiving echo signals at 6 MHz. Although the Rx transducer itself works as a band-pass filter with a center frequency of about 6 MHz and a bandwidth of interest from 4.5 MHz to 7.5 MHz (Section 2.3), it cannot significantly suppress the 3 MHz fundamental signal. As can be seen from Fig. 2.13, the Rx transducer provides an approximately 15 dB suppression at 3 MHz compared to the 6 MHz center frequency. However, the pressure of the fundamental acoustic signal is expected to be about 1~2 orders of magnitude higher than the second-harmonic signal generated due to tissue distortion, as shown by Demi et al. [4.2]. Therefore, at the input of the front-end receiver circuitry, the level of the 3 MHz fundamental signal is comparable to or even still higher than the 6 MHz second-harmonic signal. For large

input signals from the near field, the non-linearity of the LNA will introduce second-order harmonic distortion that up-converts the 3 MHz fundamental signals into the receive bandwidth (4.5 MHz ~ 7.5 MHz), resulting in signals that are mixed with the 6 MHz second-harmonic signals generated by tissue distortion.

To relieve the linearity requirement of the LNA, we've chosen to bypass the LNA at high input signal levels. The proposed configuration is shown in the signal flow diagram in Fig. 4.1. To achieve an approximately linear operation, for strong echo signals from the nearby axial depths, the LNA is bypassed. Since those signals are large enough compared to the noise level of the remaining circuitry, they can be directly fed into the input of the TGC amplifier. Compared to the open-loop LNA, the closed-loop TGC amplifier is capable of handling a wide range of signals with good gain linearity (Section 4.3.3). In the case of small signals from deeper axial depths, the LNA is connected. Since those signals are small and still fit the linear range of the LNA, harmonic distortion is no longer an important issue. Furthermore, the configuration shown in Fig. 4.1 also enables us to investigate the influence of the non-linear amplification on the image quality in future work.

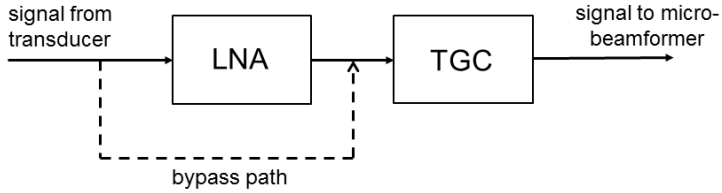



Fig. 4.1 Proposed signal flow diagram with a bypass option for the LNA.

## 4.2 Design of the Low-Noise Amplifier (LNA)

### 4.2.1 Target Specifications of the LNA

The target specifications of the prototype LNA design are listed in Table 4.1.

TABLE 4.1 TARGET SPECIFICATIONS OF THE PROTOTYPE LNA DESIGN.

| | |
|---|---|
| Technology | 0.35 μm CMOS |
| Supply voltage | 3.3V |
| Input voltage signal | • Center frequency: 6 MHz<br>• Bandwidth: 4.5 MHz ~ 7.5 MHz<br>• Estimated signal range (rms values):15 μV~100 mV |
| Gain | 20dB |
| Input-referred noise voltage* | < 15 $\mu V_{rms}$ over 3 MHz bandwidth |
| Gain variation among LNAs within a 3 × 3 group** | ±1 dB within the bandwidth 4.5 MHz ~7.5 MHz |

* The noise specification is defined to be in the order of the thermal noise of the ultrasound transducer.

** The gain mismatch specification is defined to be less than the mismatch of the transducer elements.

### 4.2.2 Topology Chosen for the LNA

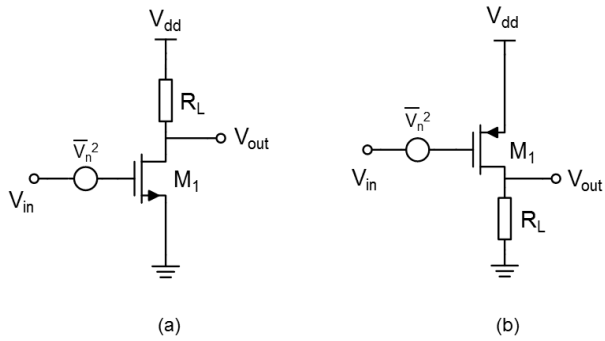



Fig. 4.2 Common-source amplifiers with a resistive load: (a) NMOS implementation , and (b) PMOS implementation.

One of the simplest open-loop amplifiers is a common-source amplifier with a resistive load. Figure 4.2 shows the circuit implementations using N-type and P-type MOSFETs. For both implementations, the voltage gains can be expressed as:

$$A = g_{m1} \cdot R_L \qquad (4.1)$$

The input referred noise power spectrum density can be expressed as:

$$\overline{V_n^2} = \frac{8}{3}kT \cdot \frac{1}{g_{m1}} + 4kT \cdot \frac{1}{g_{m1}^2 R_L} \qquad (4.2)$$

It can be seen from Eq. 4.2 that a larger transconductance ($g_{m1}$) results in a lower noise power. Since in this structure, only one transistor ($M_1$) is used, all the biasing current contributes to the transconductance ($g_{m1}$) of $M_1$. Moreover, the noise contribution of the load resistor $R_L$ referred to the amplifier input is small. Since the gain factor of this amplifier is $g_m R_L$, the noise power of the load resistor gets attenuated by a factor of $(g_m R_L)^2$ when being referred to the input, which results in an input-referred noise inversely proportional to $R_L$. Furthermore, this circuit is very compact, which is also desirable for 3D TEE application. In order to evaluate whether this circuit can meet all the design requirements mentioned in Table 4.1, prototype circuits have been fabricated and measured, which will be presented in the next section.

### 4.2.3 LNA Prototype Design

#### *Circuit Implementation*

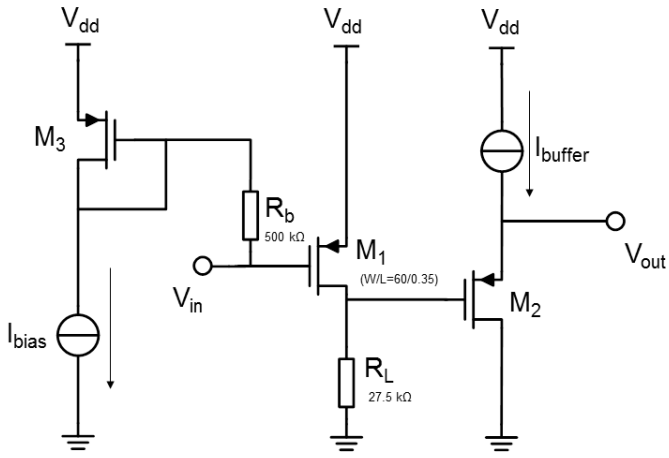



Fig. 4.3 Schematic of the LNA prototype design.

A LNA circuit has been fabricated as an auxiliary test structure on the 9-channel front-end receiver ASIC (Fig. 6.8). The schematic of the test structure is depicted in Fig. 4.3. It consists of three parts: a bias circuit ($I_{bias}$, $M_3$ and $R_b$), a main amplifier ($M_1$ and $R_L$) and an output buffer ($I_{buffer}$, $M_2$). The output buffer is used only for measurement purposes. As indicated in [4.3], a P-type MOSFET has less substrate bounce than a N-type MOSFET, because it sits in an N-well and the well junction helps to reduce the coupling of the substrate current. Therefore, we have chosen PMOS ($M_1$) as the main transistor, which is biased in the moderate inversion region. The input DC biasing voltage of the amplifier is generated by a diode-connected PMOS ($M_3$) together with a current source ($I_{bias}$), and is connected via a resistor ($R_b$) to the amplifier's input. The DC current that flows in the main amplifier branch is about 32 μA, which results in a power consumption about 105 μW under a 3.3 V supply voltage. Meanwhile, the bias circuitry consumes only 2 μW. Since the biasing resistor is much larger than the source impedance, i.e., 2.5 kΩ, the noise voltage generated by the biasing circuit is significantly attenuated when referred to the input of the amplifier and is negligible. The total simulated noise voltage is 9.6 $\mu V_{rms}$ when integrated from 4.5 MHz to 7.5 MHz.

## *Experimental Results*

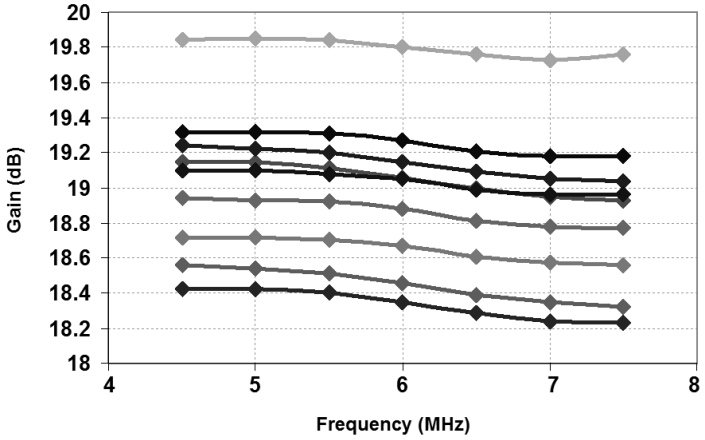



Fig. 4.4 Measured gains of 9 LNA prototypes in the signal bandwidth from 4.5 MHz to 7.5 MHz.

Figure 4.4 shows the measured gains of 9 LNA samples in the signal bandwidth from 4.5 MHz to 7.5 MHz. In this measurement, a 50 $mV_{pp}$ sinusoidal signal is applied to the input of each sample and swept across the frequency range from 4.5 MHz to 7.5 MHz. It can be seen from Fig. 4.4 that the average gain value is about 19 dB. For each prototype chip the gain roll-off is only about 0.2 dB within the bandwidth of interest. The gain variation over 9 prototype chips is within ±1 dB over the frequency range of interest.

The measured noise power spectrum density (PSD) at the buffer output is around $3.15 \times 10^{-15}$ $V^2/Hz$. Therefore, the input-referred noise PSD is about $4 \times 10^{-17}$ $V^2/Hz$ for a gain of 19 dB, which corresponds to a noise voltage of ~11 $\mu V_{rms}$ in the signal bandwidth from 4.5 MHz to 7.5 MHz.

Figure 4.5a shows the measured rms output voltages corresponding to 6 MHz input voltages swept from about 1 mV to 100 mV for one sample. Linear curve fitting is applied based on five measured datasets at small signal level (Fig. 4.5a), and a gain value of 19.55 dB is obtained. Figure 4.5b shows the gain error normalized to the gain value. It can be observed that

when the input signal level is larger than 55 mV, the gain of the LNA becomes 1 dB lower than the linear gain.

As discussed in Section 4.1, second-harmonic imaging technique has been chosen for our project. Due to the non-linear property of the LNA, the 3 MHz fundamental signals will be distorted and result in signal components at 6 MHz. To have an order-of-magnitude estimation on the influence of distortion, we assume at the input of the LNA that both 3 MHz signals and 6 MHz signals have the same amplitude. First, 3 MHz sinusoidal test signals with amplitude from about 1 mV to 100 mV (rms value) are applied. At the output of the LNA, 6 MHz signal components are detected by analyzing the signal spectrums. Next, 6 MHz sinusoidal test signals are applied to the input of the LNA and are swept with the same amplitude range. Accordingly, the 6 MHz components in the output signal spectrum are detected. Figure 4.6 shows two curves which represent the 6 MHz output signals originated from the input signals with frequencies of 3 MHz and 6 MHz, respectively. The measured output voltages are expressed in dBV units. It can be seen that under the worst-case conditions, the output 6 MHz signal contributed by the 3 MHz input signal is 20 dB less than that contributed by the 6 MHz input signal.

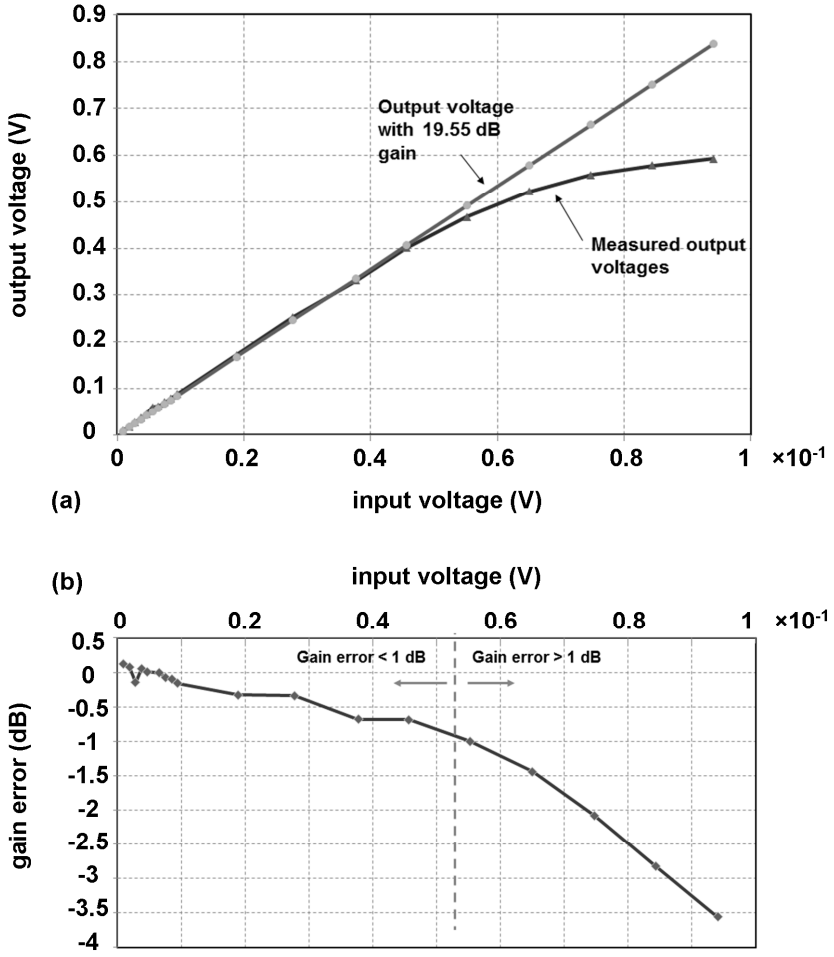



Fig. 4.5 Measurement to determine the linear amplification range: (a) the 6 MHz output voltages measured for 6 MHz sinusoidal input rms voltages from 1 mV to 100 mV, and the curve with the typical gain value, and (b) the gain error normalized to the typical value.

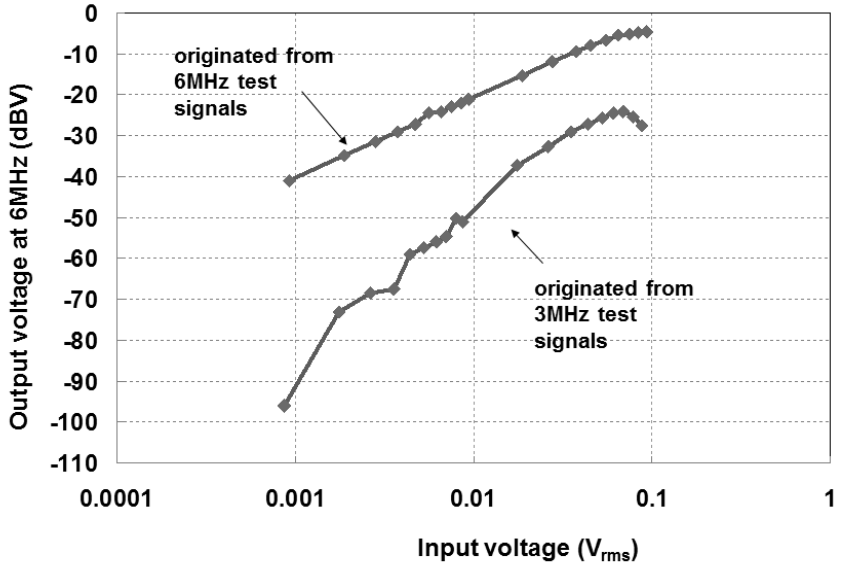



Fig. 4.6 Measured 6 MHz signal component originating from a 3 MHz test signal due to the LNA non-linearity and the 6 MHz signal originating from a 6 MHz test signal. Both 3 MHz and 6 MHz test signals have the same amplitude.

The performance of the prototype circuit is summarized in Table 4.2. It can be concluded that the proposed design fulfills the target specifications (Table 4.1).

TABLE 4.2 PERFORMANCE SUMMARY OF THE LNA PROTOTYPE.

| | |
|---|---|
| Gain | 19 dB (average)<br>Gain deviates ≥ 1 dB from the nominal value for input signal above 55 mV (rms value) |
| Input referred noise voltage | ~11 $\mu V_{rms}$ over 3 MHz bandwidth |
| Power consumption | 105 µW of the main amplifier, 2 µW of the biasing circuit |
| Gain mismatch among LNAs | Within ±1 dB for 9 chips |

## 4.3 Design of the Time-Gain-Compensation (TGC) Amplifier

### 4.3.1 Target Specifications of the TGC Amplifier

The target specifications of the TGC amplifier are listed in Table 4.3.

TABLE 4.3 TARGET SPECIFICATIONS OF THE TGC AMPLIFIER

| | |
|---|---|
| Technology | 0.35 μm CMOS |
| Supply voltage | 3.3 V |
| Gain | 0~40 dB, 4 discrete gain settings |
| Input referred noise voltage* | < 150 $\mu V_{rms}$ over the 3 MHz bandwidth |
| Input signal | • Center frequency: 6 MHz<br>• Bandwidth: 4.5 MHz ~ 7.5 MHz<br>• Input signal range (rms value)**: 150 μV ~ 1 V |
| Load capacitance*** | 250 fF |
| Power budget**** | ≈150 μW |
| Gain mismatch among TGC amplifiers within a 3 × 3 group | ±0.5 dB |

* The noise specification of the TGC is defined to be lower than the minimum output rms voltage of the LNA.

** The maximum rms signal level is expected to be less than 1 V because of the gain compression of the LNA (Fig. 4.5). In the case that for large transducer output signals the LNA can be bypassed, the maximum input signal level for TGC is expected to be less than 500 mV. The minimum rms signal level is determined by the smallest output signal level of the LNA.

*** The load capacitance is estimated based on the input capacitance of the micro-beamforming circuitry.

**** The total targeted power budget for the combined LNA-TGC amplifier is 250 μW. The LNA consumes 100 μW, thus the TGC amplifier is allocated with a power budget of approximately 150 μW.

### 4.3.2 Topology Chosen for the TGC Amplifier

There are several possible approaches reported in the literature to realize programmable discrete gain settings. For example, in [4.4], a circuit topology consisting of a resistive attenuator followed by a fixed-gain amplifier has been proposed. Different gain settings are achieved by configuring the attenuation factor of a resistor-ladder. In [4.5], a current-feedback variable gain amplifier has been presented, in which the gains are

set by the ratio of two feedback resistors. Moreover, in [4.6], a variable-gain amplifier is implemented by cascading four fixed-gain stages. A multiplexer is used to control the number of gain stages to achieve discrete gains.

For 3D TEE application, our main circuit design consideration is the power efficiency. We proposed a TGC amplifier topology, which uses local-feedback topology to achieve a high bandwidth while keeping the power consumption low [4.7]. The proposed circuit consists of a voltage-to-current (*V/I*) converter, a current-to-voltage (*I/V*) converter and a source-follower buffer. A simplified circuit diagram is shown in Fig. 4.7, where a differential circuit structure is used. The *V/I* conversion is achieved by using a differential pair ($M_{1A}$, $M_{1B}$) with source-degeneration resistor $R_S$. The *I/V* conversion is simply realized by the load resistors $R_L$. The gain of the TGC amplifier is thus defined by the resistor ratio $2R_L/R_S$. By switching between different degeneration resistors $R_{S1}$ ….$R_{S4}$, discrete gains can be achieved. In this design, we chose the gain steps to be 0 dB, 12 dB, 26 dB and 40 dB. The reason is that these values can be realized by integer resistive ratios ($2R_L/R_S$) equal to 1, 4, 20 and 100. Finally, the output differential voltages are buffered by source followers ($M_{2A}$, $M_{2B}$) to drive 250 fF loads.

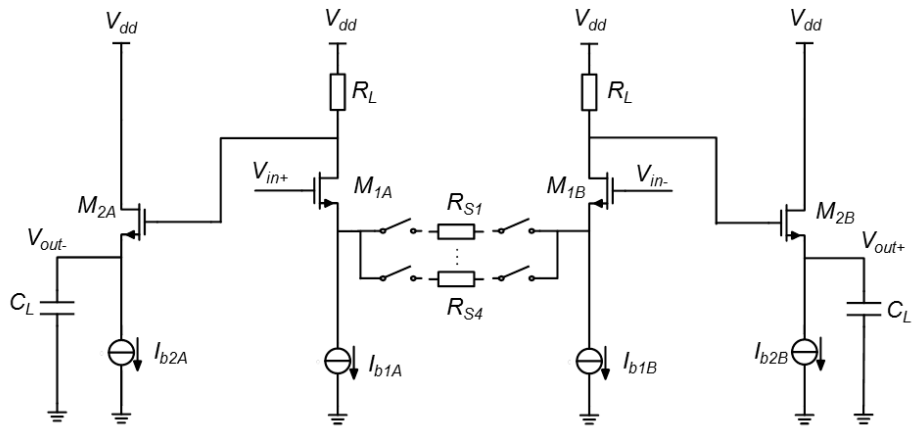



Fig. 4.7 Simplified schematic of the proposed TGC amplifier.

As described in Section 4.1, the majority of the gain-error budget has been allocated to the LNA. To ensure reasonable overall gain accuracy, the gain-error contribution o the TGC amplifier should be low enough. In our design, a cascoded-flipped-voltage-follower (CASFVF) structure [4.8] is chosen to improve the gain accuracy of the *V/I* conversion. Furthermore, errors due to the on-resistance of the switches are eliminated by using Kelvin connections.

## *CASFVF Structure*

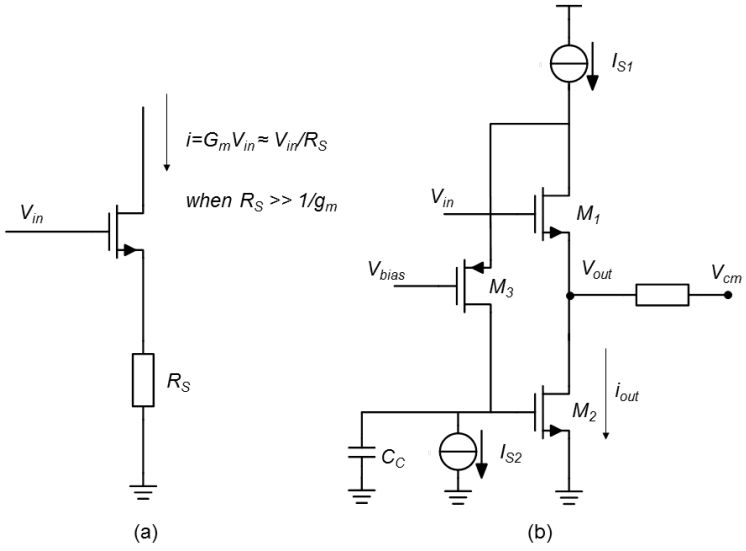



Fig. 4.8 Transconductance stages: (a) conventional trans-conductance stage with source degeneration, (b) trans-conductance stage with CASFVF.

A simple implementation of a *V/I* converter is shown in Fig. 4.8a. The equivalent transconductance $G_m$ of this common-source stage with degeneration can be written as:

$$G_m = g_m /(1 + g_m R_S) \qquad (4.3)$$

Since the transconductance $g_m$ of the NMOS transistor depends on temperature and process tolerances, an accurate *V/I* conversion is only obtained if $R_s >> 1/g_m$, leading to an equivalent transconductance:

$$G_m = 1/R_S \qquad (4.4)$$

Therefore, a high value is required for either $R_S$ or $g_m$. Considering the noise performance and chip area constraints, it is more practical to increase $g_m$ than $R_S$. The CASFVF structure is employed to realize this (Fig. 4.8b).

The CASFVF structure is essentially a voltage follower with local negative feedback. The gate terminal of $M_1$ is used as the input, and its source terminal is used as the output. $M_2$ and $M_3$ provide additional loop gain. The output conductance $g_{out}(s)$ is extremely large at DC:

$$g_{out}(0) = g_m A_L = g_m^3 r_o^2 \qquad (4.5)$$

where $A_L$ is the DC loop gain.

Since the loop gain decreases with increasing frequency, $g_{out}$(s) will decrease. Therefore, $g_{out}$(s) at the signal frequency of 6 MHz should still be large enough to maintain the accuracy of the *V/I* conversion. To achieve this with minimum power consumption, the parasitic capacitances in the CASFVF have been minimized by careful layout. To ensure stability of the loop, a compensation capacitor is added at the gate of $M_2$.

### *Degeneration Resistor Network with Kelvin Connections*

The switches in the degeneration resistor network are implemented by MOSFETs operating in the linear region. Their on-resistance is signal-dependent and sensitive to process, supply-voltage and temperature variations. To prevent the resulting loss of gain accuracy, Kelvin connections are used. As shown in Fig. 4.9, the currents flowing through switches $SW_1$ and $SW_2$ are DC constants, which are defined by the current sources $I_{S1A}$, $I_{S1B}$ and the current sinks $I_{S2A}$, $I_{S2B}$. There is no signal current

flowing in $SW_1$ and $SW_2$. As a result, the signal voltage is accurately copied to the two terminals of the degeneration resistor $R_S$. In the meantime, $R_S$, $SW_3$, $M_{2A}$, $M_{2B}$, $SW_4$ form the signal-current loop. Since $SW_3$ and $SW_4$ are in series in the loop, their ON-resistance does not affect the accuracy of the output current.

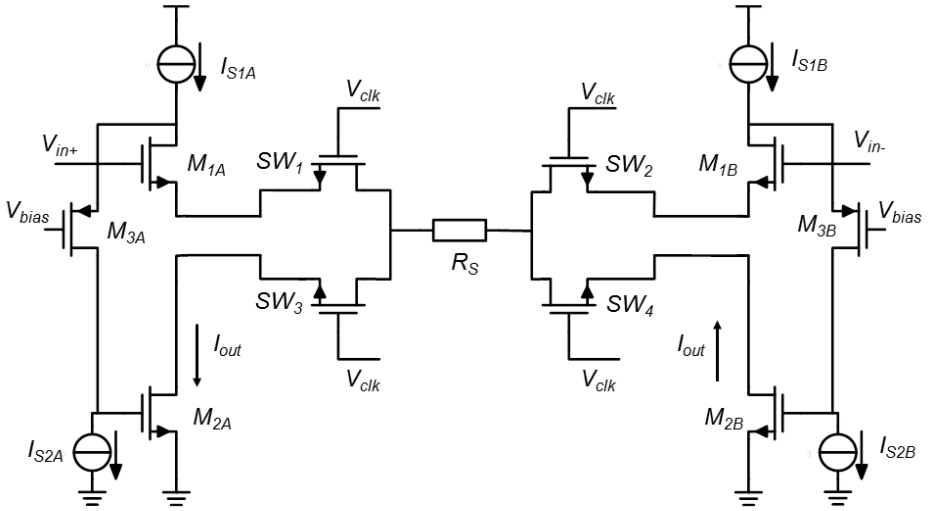



Fig. 4.9 Degeneration resistor network with Kelvin switches.

After employing the CASFVF structure and Kelvin connections, the equivalent trans-conductance $G_{diff}$ of the differential *V/I* converter can be expressed as:

$$G_{diff} = 2 / R_S \qquad (4.6)$$

Consequently, the differential output current $I_{out}$ is:

$$I_{out} = G_{diff} V_{in} = 2V_{in} / R_S \qquad (4.7)$$

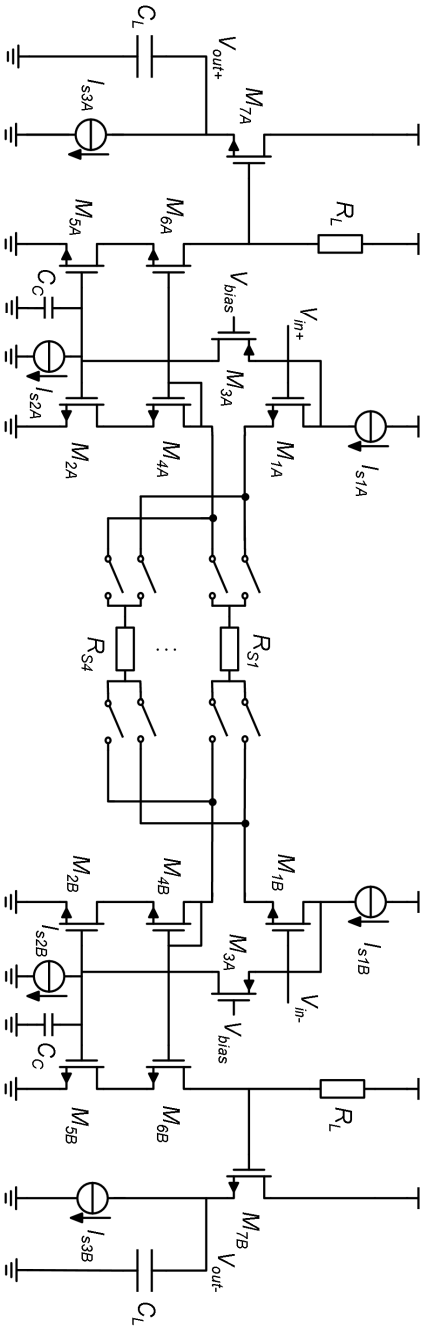



Fig. 4.10 Complete schematic of the TGC amplifier.

### *Current-to-Voltage (I/V) Conversion and Buffering*

To realize the *I*/*V* conversion, the currents generated by the *V*/*I* converter are copied to the output branches by current mirrors and flow into the load resistors $R_L$ (see Fig. 4.10). To reduce current-copying errors due to the channel-length modulation, cascoded current mirrors are used ($M_{5A,}$ $M_{6A}$, $M_{5B}$, $M_{6B}$). Transistors $M_{4A}$ and $M_{4B}$ are inserted in the CASFVF structure to keep the mirror balanced. To drive the 250 fF loads, differential signal voltages across the load resistors $R_L$ are buffered by a unity-gain source follower. Finally, the gain of the amplifier can be written as:

$$Gain = 2R_L / R_S \qquad (4.8)$$

Fig. 4.11 shows the simulated small-signal gain of the TGC amplifier as a function of frequency for the four gain settings.

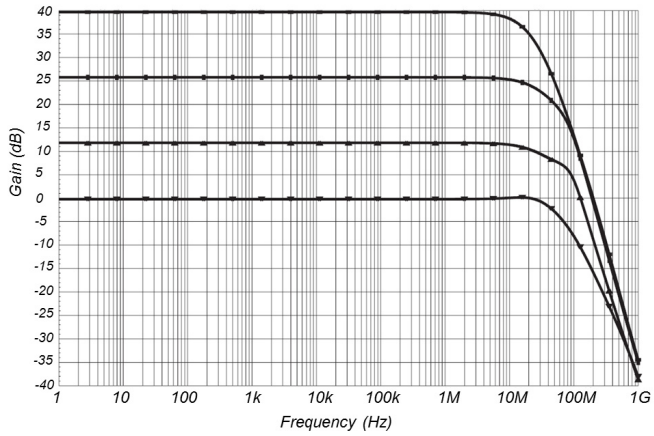



Fig. 4.11 AC analysis of the TGC amplifier for gain settings of 0 dB, 12 dB, 26 dB and 40 dB.

## 4.3.3 TGC Amplifier Prototype Design

A prototype TGC amplifier has been fabricated in a standard 0.35 μm CMOS technology. Figure 4.12 shows the die micrograph along with a picture of the circuit layout, which is not visible in the micrograph due to the metal coverage. The core area of the TGC amplifier is 0.29 × 0.25 $mm^2$.

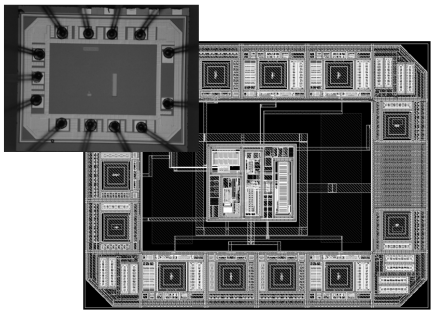


Fig. 4.12 Die micrograph and layout of the prototype TGC amplifier.

Figure 4.13 shows the measured gains of 11 TGC amplifiers in the signal bandwidth from 4.5 MHz to 7.5 MHz for the 4 different gain settings. The sample-to-sample gain variation is within ±0.5 dB for all the settings. It can also be observed that the gain roll-off from 4.5 MHz to 7.5 MHz is within 3 dB for all the settings. Since this value is much smaller than the roll-offs of the transducer elements themselves in the bandwidth of interest (Fig. 2.13), it will not significantly degrade the image quality.

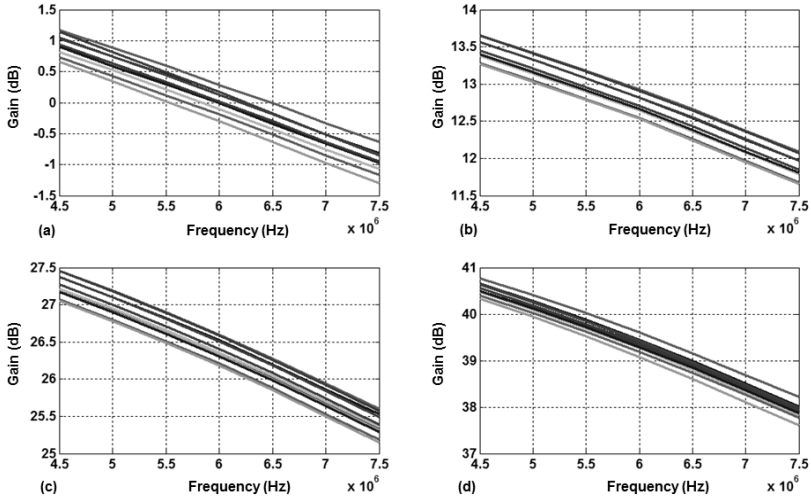



Fig. 4.13 Measured gains of 11 TGC amplifiers in the signal bandwidth from 4.5 MHz to 7.5 MHz for 4 different gain settings: (a) 0 dB setting, (b) 12 dB setting, (c) 26 dB setting, and (d) 40 dB setting.

The measured noise power spectral density (PSD) at the output of the TGC amplifier is $5 \times 10^{-12}$ $V^2$/Hz at the 40 dB gain setting. This corresponds to an input-referred noise PSD of ~ $5\times 10^{-16}$ $V^2$/Hz and a noise voltage of less than 50 $\mu V_{rms}$ in the signal bandwidth from 4.5 MHz to 7.5 MHz. The experiment shows that the circuit has a wide linear amplification range for signals from the noise floor to around 1 V (rms value) with gain errors of less than 0.5 dB. It consumes only 130 μW when driving 250 fF loads. Table 4.4 summarizes the circuit performance.

TABLE 4.4 PERFORMANCE SUMMARY OF THE TGC AMPLIFIER PROTOTYPE

| | |
|---|---|
| Gain | 4 settings (0/12/26/40 dB) |
| Gain mismatch among TGCs | < ±0.5 dB within the bandwidth from 4.5 MHz to 7.5 MHz |
| Input referred noise voltage | <50 $\mu V_{rms}$ over 3 MHz bandwidth |
| Input signal dynamic range | ~60 dB, from noise floor to ~1 V (rms value) |
| Chip area | $0.29 \times 0.25$ $mm^2$ |
| Power consumption | 130 μW for 250 fF loads |

## 4.4 Conclusions

This chapter has presented the circuit implementations of the LNA and the TGC amplifier for application in 3D TEE. We have focused on the LNA and TGC amplifier co-design in order to obtain a low-power solution. Integrated prototypes of an LNA and a TGC amplifier have been manufactured in a 0.35 μm CMOS technology and tested.

The LNA is chosen to be a simple open-loop single-ended amplifier. The prototype chips have a measured average gain of 19 dB with a bandwidth large enough to handle signals from 4.5 MHz to 7.5 MHz. The gain variation of 9 samples is within ±1 dB over the bandwidth of interest, which is below the sensitivity variation of the transducer elements. The input-referred noise voltage is about 11 $\mu V_{rms}$ integrated over the bandwidth-of-interest, which meets the design specification. The LNA core consumes only 105 μW. One disadvantage of the simple LNA is its non-linearity. Measurements show that when the input signal reaches about 55 mV (rms value), the gain deviates 1 dB from the nominal value. Since the second-harmonic imaging

technique will be used in the project — one concern is that the large 3 MHz fundamental signal will be distorted due to the non-linearity of the LNA and result in a 6 MHz signal component. Experimental results show that the 6 MHz signal component originating from a 3 MHz test signal is 20 dB smaller than the 6 MHz signal originated from a 6 MHz test signal, under the assumption that both 3 MHz and 6 MHz test signals have the same amplitude. The influence of the LNA non-linearity on the image quality will be a topic for future research. At this moment, we can bypass the LNA for large input signals if necessary.

The TGC amplifier can provide gains of 0 dB, 12 dB, 26 dB and 40 dB. The measured chip-to-chip gain variation of 11 samples is less than ±0.5 dB for all gain settings. The measured input-referred noise voltage integrated from 4.5 MHz to 7.5 MHz is less than 50 $\mu V_{rms}$, which is lower than the expected minimum output signal level of the LNA. Furthermore, the TGC amplifier has a wide input dynamic range of about 60 dB and consumes only 130 μW when driving a 250 fF load.

The LNA and the TGC amplifier designs presented in this chapter are low-power and compact. They are the important building blocks for the front-end receive signal processing chain. In the next chapter, the design of the third building block — the low power micro-beamforming circuitry — will be described.

## 4.5 References

[4.1] P. E. Allen, D. R. Holberg, *CMOS Analog Circuit Design*, Oxford University Press, 2002.

[4.2] L. Demi, M. D. Verweij, N. de Jong, K. W. A. van Dongen, "Modeling nonlinear acoustic wave fields in media with inhomogeneity in the attenuation and in the nonlinearity", *Proceedings IEEE Ultrasonics Symposium*, 2010, pp. 2056-2059.

[4.3] A. Helmy, M. Ismail, *Substrate Noise Coupling in RFICs*, New York: Springer, 2008.

[4.4] E. Brunner, "An ultra-low noise linear-in-dB variable gain amplifier for medical ultrasound applications", Conference Record. *Microelectronics Communications Technology Producing Quality Products Mobile and Portable Power Emerging Technologies*, pp.650-655, 1995.

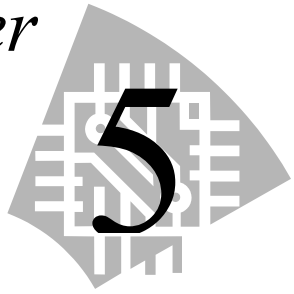
[4.5] D. Ma, C. Zhang, H. Chao, M. Koen, "Integrated low-power CMBF-free variable-gain amplifier for ultrasound diagnostic applications", *Analog Integrated Circuits and Signal Processing*, vol. 61, pp. 171-179, 2009.

[4.6] M. Sawan, R. Chebli, K. Kassem, "Integrated front-end receiver for a portable ultrasonic system", *Analog Integrated Circuits and Signal Processing*, vol. 36, pp. 56-67, 2003.

[4.7] J. Yao, Z. Yu, M. A. P. Pertijs, G. C. M. Meijer, C. T. Lancée, J. G. Bosch, N. de Jong, "Design of a low power time-gain-compensation amplifier for a 2D piezoelectric ultrasound transducer", *Proceedings IEEE Ultrasonics Symposium*, 2010, pp. 841-844.

[4.8] J. Ramirez-Angulo, S. G .I. Padilla, R. G. Carvajal, A. Torralba, M. Jiménez, F. Muňoz, "Comparison of conventional and new flipped voltage structure with increased input/output swing and current sourcing/sinking capabilities", *IEEE International Midwest Symposium on Circuits and Systems*, 2005, pp. 1276-1291.

# *Micro-Beamformer Design*




The beamforming principle is based on delaying the signals received by different transducer elements relative to each other in such a way that the signals received from the focal point are aligned in time and can be coherently summed. In Chapter 3, we have proposed a micro-beamforming scheme for 3D TEE and the associated design requirements have been derived. In this chapter, we focus on the circuit implementation. In principle, a micro-beamformer can either be implemented in the analog domain or in the digital domain. For our specific application, analog beamforming is chosen and the reason is given in Section 5.1. Section 5.2 presents various approaches to realize analog delays. The so-called "pipeline-operated sampled delay" principle has been chosen. Based on this principle, a pipeline-operated S/H delay structure is introduced. This structure gives better performance in terms of timing accuracy, gain accuracy, power consumption and flexibility, compared to other delay line structures. In Section 5.3, signal summation methods in the voltage, current and charge domains are briefly described. In Section 5.4, we present two prototype designs with the same delay line topology but different signal summation methods. Their performances are thoroughly evaluated. We summarize this chapter in Section 5.5.

## 5.1 Design Choice: Digital Beamforming vs. Analog Beamforming

Before we dive into the transistor-level design, a choice must be made between digital beamforming and analog beamforming. Figure 5.1a shows an ultrasound receive-signal processing chain with digital beamforming applied. Digital beamforming offers the advantage of being more precise. Once the data is digitized, digital delays and summation can be flexibly applied. However, as can be seen from Fig. 5.1a, digital beamforming requires an analog-to-digital converter (ADC) for each transducer element. Typical ADCs for ultrasound application run at about 20~50 Mega-Samples-per-Second (MSPS) with an 8~12-bit resolution [5.1][5.2][5.3][5.4]. The typical power consumption of commercially available ultrasound receive front-end ICs, which include LNAs, TGC amplifiers and ADCs, is in the order of 100 mW per channel [5.2][5.3][5.4]. Moreover, for channel-count reduction purposes, after analog-to-digital conversion, extra digital circuits, including e.g. memories and digital adders, are still indispensable in providing appropriate delays to those digitized signals and summing them up. These digital circuits consume power as well. As reported in [5.5], even when employing a low-power design strategy, the digital circuits still consume about 450 mW for 16 channels with a clock frequency of 40 MHz. For 3D TEE application, in which ultrasound signals from more than 2000 transducer elements must be processed simultaneously, digital beamforming is not suitable mainly due to its unacceptably large power consumption. Therefore, in our design, analog beamforming is employed (Fig. 5.1b). Many analog beamformers with different structures have been reported in literature [5.6][5.7][5.8][5.9][5.10][5.11][5.12]. For example, in [5.6] presented a four-channel beamformer with 3.2 mW power consumption is presented, which already shows a reduction in power consumption of two orders of magnitude per channel compared to digital implementations. Later in this chapter, we explore ways to design an analog beamformer with improved power efficiency which delivers good performance in terms of accuracy and flexibility.

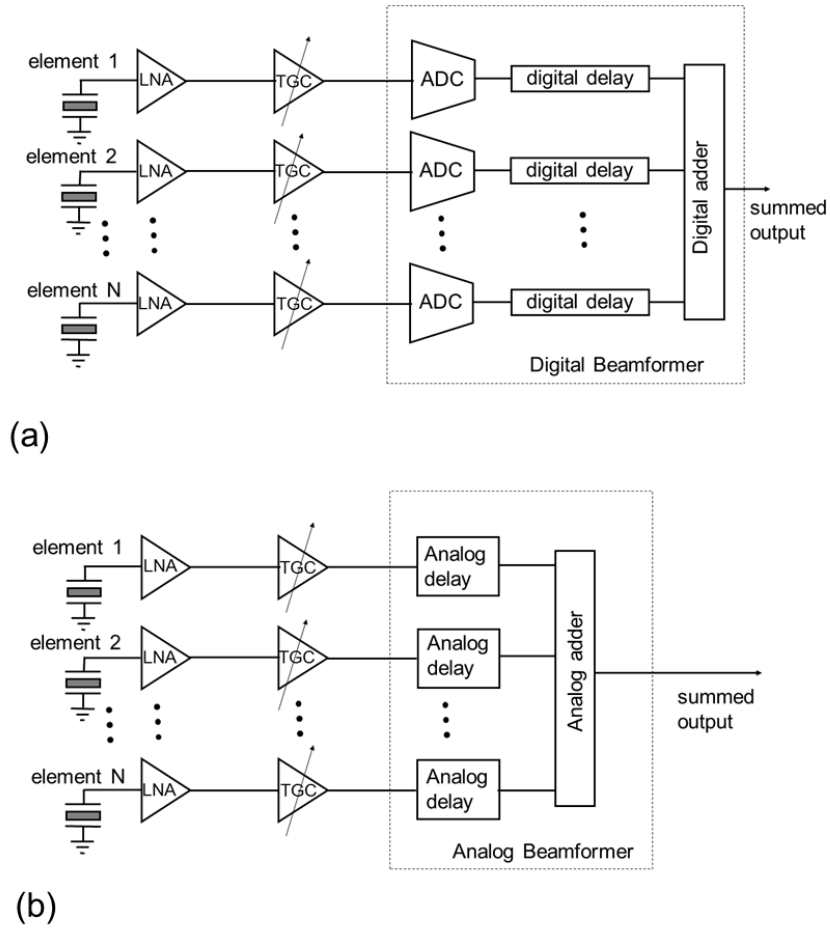



Fig. 5.1 Beamforming implementation: (a) digital beamforming, (b) analog beamforming.

## 5.2 Analog Delay Line Architectures

### 5.2.1 Possible Approaches

There are various circuits that are capable of generating analog delays for ultrasound applications. We restrict ourselves to those circuit solutions that are suitable for monolithic integration. One widely used approach is based on cascading all-pass filter cells [5.6][5.7][5.8][5.9]. The all-pass filter cell is

required to achieve a constant group delay (i.e., a linear phase response with frequency) [5.13]. Thus, by cascading a chain of all-pass filter cells, a delay range with a step size equal to the group delay of a single cell can be achieved. There are two main limitations to this approach. Firstly, because of the cascading, the gain errors associated with these filter cells accumulate and result in different gains for different delay settings. Secondly, once the group delay for an all-pass filter cell is fixed, it is difficult to modify. Even with a tunable filter cell [5.9], the tuning range is rather limited. Therefore, this design approach shows poor adaptability.

An alternative approach to generate analog delays is based on charge-coupled devices (CCD) [5.14] or bucket-brigade devices (BBD) [5.10][5.11]. The CCD-type delay lines are difficult to implement in a standard CMOS process. The BBD-type delay lines are CMOS compatible, but have the problem that passing charges through a number of their delay stages would result in delay-dependent transfer functions.

In [5.15][5.16][5.12], an analog delay line using the so-called "pipelined-sampled delay" principle has been proposed. This approach is also known as the analog RAM delay [5.17], or the time-interleaved S/H delay [5.18]. The input signals are sampled and stored in a so-called analog first-in first-out (AFIFO) memory. The AFIFO can be implemented either in the voltage domain [5.15] using S/H stages, or in the current domain [5.12] using switched-current cells. Every sample is held for a certain time before being released to the output. Since this delay time is defined by a digital clock, good timing accuracy can be achieved. The use of parallel sampling operation, in contrast with cascaded delay line structures, ensures a delay-independent transfer function. In our design, we have adopted the principle of pipelined-sampled delay and have chosen to implement the AFIFO with S/H stages. This is described in the following section.

### 5.2.2 Chosen Approach: Pipeline-Operated S/H Delay Line

The working mechanism of a pipeline-operated S/H delay line is depicted in Fig. 5.2 for the simple case that a single-ended circuit is used. There are two groups of clock signals: group A ($\phi_1$ to $\phi_N$) and group B ($\phi_{1d}$ to $\phi_{Nd}$). In this

example, $N=8$. The pulse width is $\Delta t$. Within a group, the clock signals control the analog switches to be cyclically closed. Meanwhile, there is a relative time delay between group A and group B, which can be written as:

$$\tau = k\,\Delta t \qquad (5.1)$$

where $k$ is an integer. In the example in Fig. 5.2, $k$ is 3.

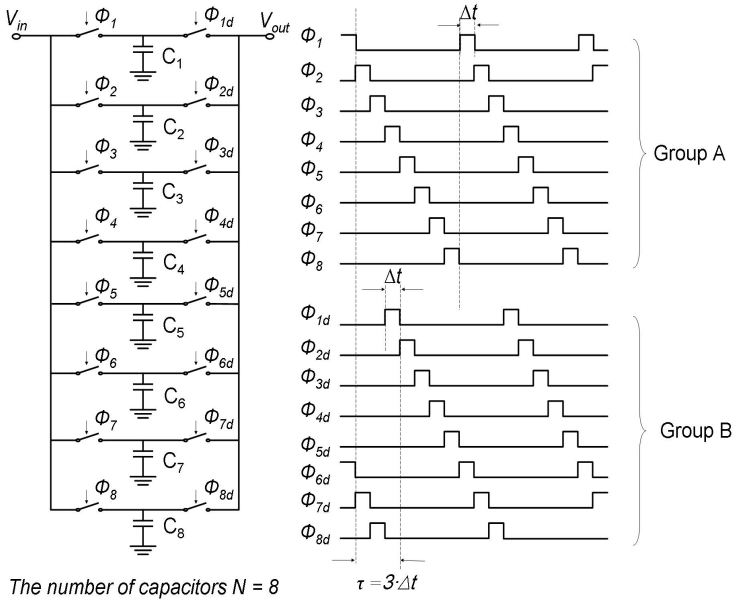



Fig. 5.2 Pipeline-operated S/H delay line.

The input voltage signal is cyclically sampled. The values of $N$ of such samples are sequentially stored on capacitor pairs $C_1$ to $C_N$, respectively. This process is then repeated for the next group of $N$ samples. Every sample is kept for a certain time before being released to the output. The sampling frequency must obey the Nyquist law in order to recover the signal information from the samples. Moreover, the pulse width $\Delta t$ should be long enough for the signal to settle. Besides, if we define the largest achievable time delay to be:

$$\tau_{max} = k_{max}\,\Delta t \qquad (5.2)$$

we should make sure that the capacitor voltage is read out before a new sample is taken. Therefore, $k_{max}$ is determined by the number of capacitors $N$ in the delay line, and can be written as:

$$k_{max} = N - 1 \qquad (5.3)$$

The pipeline-operated S/H delay line offers several advantages that make it a suitable circuit block to be used for 3D TEE:

- **Low power consumption:** In this delay structure, S/H stages virtually consume no power. Only the digital control circuits contribute significantly to the power consumption. Compared to e.g. filter-based delay structures [5.6] or switched-current delay cells [5.12], this delay structure has no active analog circuits, and as a result, delivers a better power efficiency.
- **High accuracy:** The delay step size is defined by the digital clock. Thus, good timing accuracy can be achieved. The use of parallel S/H stages ensures a delay-independent gain.
- **High flexiblity:** The delay step size and range can easily be adjusted by tuning the clock frequency.

There are also a number of nonidealities to be considered that must be addressed by careful design, such as: undesired charge injection error, *kT/C* noise, mismatch of capacitors. These will be discussed in section 5.4.

## 5.3 A Brief Overview of Signal Summation Methods

To complete the beamforming function, delayed signals from various transducer elements must be added up. The summation can be done in the voltage domain [5.15]. This approach typically involves an operational amplifier and extra circuit components. Instead of summing the signals in the voltage domain, in [5.12] a switched-current delay line has been presented, in which current-domain summation is performed. However, since the piezo-electric transducers typically used in an ultrasound system produce an output in the voltage domain by nature, the current-mode operation requires extra circuitry for voltage-to-current (V/I) conversion. As explained by the authors in [5.12], the linearity and bandwidth of the V/I

converter are very challenging design aspects. The advantage of the in-current-domain summation is its simplicity, as it only requires tying the outputs of the V/I converters together. In Section 5.4.2, we present an analog beamformer prototype that employs the current domain summation concept. Alternatively, signal summation can be done in the charge domain [5.19]. Later, in Section 5.4.3, we will prove that the charge-mode summation method combined with the pipeline-operated S/H delay structure intrinsically leads to circuits with even lower complexity and higher power efficiency than the current-mode summation method.

## 5.4 Prototype Designs

### 5.4.1 General Design Requirements and Goals

In Chapter 3, we have presented a micro-beamforming scheme that employs "pre-steering" (Section 3.3). The design requirements to readout transducer elements in 3 × 3 sub-groups have been derived and listed in Table 3.3. Though the ideal delay times differ for elements located in the center, side-middle and corner (see Fig. 3.9), for simplicity reasons, we decided to make the delay ranges for all the elements equal with a maximum value of 280 ns (Section 3.2). Thus, the same circuit implementation and layout can be used for all elements. The general design specifications for a micro-beamformer design are summarized in Table 5.1.

In this section, we present two prototype designs. The first prototype is a micro-beamforming cell with a pipeline-operated S/H delay line and a V/I converter for current-mode summation. The second prototype is a 9-channel beamformer that employs the same delay principle but with signal summation in the charge domain. The goals of the designs are threefold. The first goal, as described in Section 5.2, is to demonstrate from an architectural perspective that the use of a pipeline-operated S/H delay circuit leads to higher power efficiency, and better accuracy and flexibility compared to other delay line architectures. There is little information on real silicon realizations in open literature. Thus, by measuring prototype chips we can

evaluate the circuit performance and prove the effectiveness of the design. Secondly, the two prototypes employ different signal summation methods. This allows us to make a performance comparison. Thirdly, we can identify the error sources that limit the precision, which will help to gain insight for future improvement.

TABLE 5.1 GENERAL TARGET SPECIFICATIONS FOR THE MICRO-BEAMFORMER

| | |
|---|---|
| Technology | 0.35 μm CMOS |
| Supply voltage | 3.3 V |
| Number of inputs | 9 |
| Features of input signals | • Center frequency: 6 MHz<br>• Bandwidth: 50% (4.5 MHz ~ 7.5 MHz) |
| Delay step size | 40 ns |
| Programmable delay range* | 0 ns (without S/H operation)<br>40 ns ~280 ns (with S/H operation) |
| Gain variations within a 3 × 3 group | < ±0.5 dB |
| Input-referred noise voltage** | ~ 1 $mV_{rms}$ |
| Input signal dynamic range | ~ 60 dB |
| Power consumption*** | < 500 μW per channel |

* For 0 ns delay setting, there is no S/H operation, since the input switch and the output switch associated with each capacitor open or close simultaneously. The input signal of the delay line can be treated as passing through an RC filtering network.

** The input-referred noise level of the micro-beamformer must be lower than the minimum output signal level of the TGC amplifier, which is expected to be about 5 mV (rms value). We set the target for the input-referred noise voltage to be about 1 $mV_{rms}$ as the design target.

*** As described in Chapter 4, the power consumption of the LNAs and TGC amplifiers amounts to 250 μW per channel. In order to keep the total power consumption of the ASIC with about 2000 channels within the range of 1~2 W, we set the power budget of the micro-beamformer to be less than 500 μW per channel.

### 5.4.2 Precision Considerations of the Pipeline-Operated S/H Delay Structure

The pipeline-operated S/H delay structure shown in Fig. 5.2 suffers from charge injection and clock feed-through errors [5.20]. To mitigate these errors, differential structures could be used. It is worth noting that the use of differential structures only gives a first-order error reduction. The residual

charge-injection error is mainly caused by transistor threshold-voltage mismatch, mismatch of sampling capacitors, and the body effect of the switch transistors. Meanwhile, sampling-capacitor mismatch and switch-transistor mismatch contribute to the residual clock-feed-through error. In addition to the aforementioned residual errors, the sampling circuit suffers from *kT/C* noise [5.20]. All the above aspects must be taken into account during the designing process to make sure the design specifications can be met.

### *Residual Charge Injection Error*

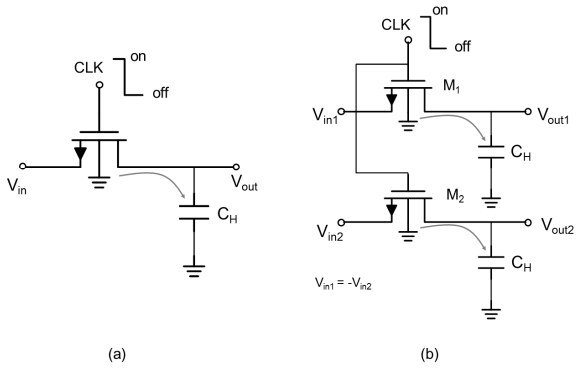



Fig. 5.3 Illustration of the charge injection error: (a) single-ended S/H circuit, (b) differential S/H circuit.

Figure 5.3a depicts a simple sampling circuit. The sampling switches are driven between $V_{dd}$ and $V_{ss}$. The total channel charge of the switches can be expressed as [5.20]:

$$Q_{ch} = WLC_{ox}(V_{dd} - V_{in} - V_{TH0} - \gamma\sqrt{2\phi_B + V_{in}} + \gamma\sqrt{2\phi_B}) \tag{5.4}$$

For the worst-case estimation, we assume that the entire channel charge is injected onto the sampling capacitor $C_H$ when the MOS switch turns off. The injected charge causes an error voltage at the output which can be written as:

$$\Delta V = \frac{Q_{ch}}{C_H} = \frac{WLC_{ox}(V_{dd} - V_{in} - V_{TH0} - \gamma\sqrt{2\phi_B + V_{in}} + \gamma\sqrt{2\phi_B})}{C_H} \tag{5.5}$$

The switch is the minimum-size N-type MOSFET with a width and length equal to 0.5 μm and 0.35 μm, respecitively. The transistor model parameters $V_{TH0}$, $\gamma$, $C_{ox}$, and $\varphi_B$ are 0.6 V, 0.55 $V^{1/2}$, 4.9 × $10^{-3}$ F/$m^2$ and 0.43 V, respectively. The sampling capacitor has an area of 170 $\mu m^2$ and a capacitance of 250 fF. We assume $V_{dd}$ is 3.3 V and $V_{in}$ has a minimum level of 0.8 V. Using Eq. 5.5, the error voltage can be calculated, which is about 6 mV, and is too large to be accepted in our application.

Now we will consider the differential sampling circuit as shown in Fig. 5.3b. Assume that $W_1L_1 = W_2L_2 = WL$, and the zero-biased-threshold voltage ($V_{TH0}$) of the MOS switch $M_2$ has a mismatch of $\Delta V_{th}$ compared to the zero-biased-threshold voltage of $M_1$, while the sampling capacitor in the negative path has a mismatch of $\Delta C_H$ compared to $C_H$. The residual error voltage can then be expressed as:

$$\begin{aligned}\Delta V_{residual} &= \Delta V_1 - \Delta V_2 \\ &= \frac{WLC_{ox}(V_{dd} - V_{in1} - V_{TH0} - \gamma\sqrt{2\phi_B + V_{in1}} + \gamma\sqrt{2\phi_B})}{C_H} \\ &- \frac{WLC_{ox}[V_{dd} - V_{in2} - (V_{TH0} + \Delta V_{TH}) - \gamma\sqrt{2\phi_B + V_{in2}} + \gamma\sqrt{2\phi_B}]}{C_H + \Delta C_H}\end{aligned} \tag{5.6}$$

From Eq. 5.6, four error terms can be identified. Their features are summarized in Table 5.2 together with order-of-magnitude estimations of the resulting error voltages based on the model parameters of the chosen 0.35 μm CMOS process. The transistor model parameters used in this calculation are the same as those used in the single-ended case (Eq. 5.5). The estimated MOSFET threshold-voltage mismatch $\Delta V_{th}$ is ±75 mV (±3σ value)[1]. All the sampling capacitors have an area of 170 $\mu m^2$ and a

[1] For the chosen 0.35 μm CMOS process, the MOSFET matching coefficient is calculated for devices with L ≥ 2 μm. For shorter channels, the matching behavior is deteriorated by extra mismatch causes such as source series resistance and short/narrow channel effects. To have a safety margin, we chose ±3σ for the minimum size transistors in calculation.

capacitance of 250 fF. The mismatch among capacitors ($\Delta C_H/C_H$) is estimated to be ±0.3% (±3σ value)[1].

Based on the analysis shown in Table 5.2, errors due to residual charge injection amount to an error voltage level of about 1 mV to 2 mV, if the gain error is neglected.

[1] This value is recommended by the design manual of the chosen 0.35 μm CMOS process to have a safety margin for mismatch-error estimation.

TABLE 5.2 RESIDUAL CHARGE INJECTION ERROR: CAUSES, FEATURES AND ESTIMATION

| Cause | Error Term | Feature | Order-of-magnitude Estimation of Error Voltages* |
|---|---|---|---|
| Mismatch in overdrive voltages of the switches | $-\frac{WLC_{ox}}{C_H}(V_{in1}-V_{in2})$ | gain error | ≈ 0.35% (Since the micro-beamformer is allocated with a gain error budget of ±0.5 dB. This error term is negligible.) |
| Mismatch of the zero-body-bias threshold voltages $V_{th0}$ | $\frac{WLC_{ox}}{C_H}\cdot\Delta V_{th}$ | Offset error | ±260μV |
| Non-linearity due to the body effect | $-\frac{WLC_{ox}\gamma}{C_H}(\sqrt{2\varphi_B+V_{in1}}-\sqrt{2\varphi_B+V_{in2}})$ | Signal-dependent error and non-linear | Error proportional to signal swing about -1 mV for 1V signal swing |
| Mismatch of sampling capacitors | $\frac{WLC_{ox}\gamma\cdot(\Delta C_H/C_H)}{C_H}\cdot V_{overdrive}$ | Signal-dependent error | ±10 μV (for an overdrive voltage of 1 V) |

- Calculations were based on the model parameters of the N-type MOSFET and metal-insulator-metal (MIM) capacitor in the chosen 0.35μm CMOS process.

### *Residual Clock Feed-through Error*

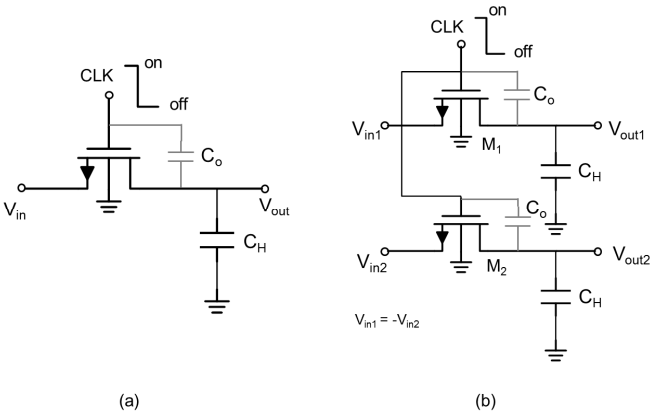



Fig. 5.4 Illustration of clock feed-through error: (a) single-ended S/H circuit, (b) differential S/H circuit.

Clock feed-through errors are caused by capacitive coupling of the clock transitions to the sampling capacitor via the gate-drain or gate-source overlap capacitors. The voltage error for the simple sampling circuit shown in Fig. 5.4a can be written as:

$$\Delta V = V_{dd} \frac{C_o}{C_o + C_H} \tag{5.7}$$

For the differential case (Fig. 5.4b), mismatches of both sampling capacitors $C_H$ and overlapping capacitors $C_o$ contribute to the residual clock feed-through error. Firstly, if we assume the overlapping capacitance $C_o$ is a constant and the sampling capacitor in the negative path has a mismatch of $\Delta C_H$ compared to $C_H$ , then the residual error voltage can be expressed as:

$$\Delta V_{residual} = V_{dd} \left( \frac{C_o}{C_H + C_o} - \frac{C_o}{C_H + \Delta C_H + C_o} \right) \tag{5.8}$$

The overlap capacitance can be calculated using the following equation:

$$C_O = C_{gdo} \cdot W \tag{5.9}$$

where $C_{gdo}$ is the gate-drain overlap capacitance of unit width (unit: F/m), and W is the width of the MOSFET. In the NMOS model of the chosen 0.35 μm CMOS process, $C_{gdo}$ has a typical value of $1.68 \times 10^{-10}$ F/m. For W=0.5μm, $C_o$ is about $8.4 \times 10^{-17}$ F. If $C_H$, $\Delta C_H/C_H$ and $V_{dd}$ are equal to 250 fF, ±0.3 % and 3.3 V, with a single-ended structure, using Eq. 5.7, the error voltage is about 1 mV. Using a differential structure, the residual clock feed-through error due to the mismatch of sampling capacitors has an estimated order-of-magnitude of ± 3.3 μV.

Next, if we assume the sampling capacitors are well matched and the overlapping capacitor in the negative path has a variation of $\Delta C_o$ compared to $C_o$, then the residual error voltage can be expressed as:

$$\Delta V_{residual} = V_{dd}\left(\frac{C_O}{C_H + C_O} - \frac{C_O + \Delta C_O}{C_H + C_O + \Delta C_O}\right) \qquad (5.10)$$

In the NMOS model of the chosen 0.35 μm CMOS process, $C_{gdo}$ varies between $1.58932 \times 10^{-10}$ F/m and $1.7707 \times 10^{-10}$ F/m[1], with a typical value of $1.68 \times 10^{-10}$ F/m. We assume all the switches have an equal width of 0.5 μm, and that $C_H$ and $V_{dd}$ are equal to 250 fF and 3.3 V, respectively. Using Eq. 5.10, the residual clock feed-through error due to the mismatch of the overlapping capacitors has an estimated order-of-magnitude of ±60 μV.

***kT/C Noise***

The sampling circuits in the pipeline-operated delay line introduce *kT*/*C* noise. With 250 fF sampling capacitors[2], an input-referred noise voltage of about 200 $\mu V_{rms}$ is expected for the differential S/H circuit.

Table 5.3 summarizes the aforementioned three error sources and their estimated error magnitude based on the chosen 0.35 μm CMOS process and the chosen circuit parameters. It can be seen that the residual charge

[1] These are the worst-case corner values.

[2] This is the minimum-size capacitor that fulfills the matching requirement in the chosen 0.35 μm CMOS process.

injection is the dominant error source. Since the total error fulfills the noise requirement, it is sufficient to keep the simple differential S/H structure without adding extra circuits to improve the accuracy.

TABLE 5.3 SUMMARY OF ERROR SOURCES AND THEIR ESTIMATED ERROR MAGNITUDE

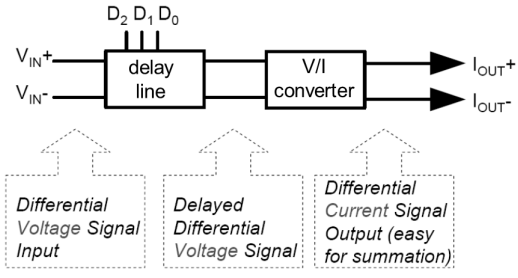
| Error Source | Estimated Magnitude |
|---|---|
| Residual charge injection | 1 mV ~ 2 mV |
| Residual clock feed-through | < 100 μV |
| *kT*/*C* noise | < 200 $\mu V_{rms}$ |

***Layout Considerations***

During the layout design, special attention is necessary to optimize capacitors matching. Parasitic capacitance must be minimized. Moreover, since there are many clock signals involved in the micro-beamforming circuit, on-chip shielding of clock lines is required to minimize clock-to-clock and clock-to-signal coupling.

### 5.4.3 Prototype I: A Micro-Beamforming Cell with a Pipeline-Operated S/H Delay Line and a V/I Converter

***Micro-Beamforming Cell Implementation***




| $D_2$ | $D_1$ | $D_0$ | Delay Time (ns) |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | 40 |
| 0 | 1 | 0 | 80 |
| 0 | 1 | 1 | 120 |
| 1 | 0 | 0 | 160 |
| 1 | 0 | 1 | 200 |
| 1 | 1 | 0 | 240 |
| 1 | 1 | 1 | 280 |

Fig. 5.5 Block diagram of the micro-beamforming cell.

In this section, the design of a micro-beamforming cell that is used to construct micro-beamformers is described [5.21]. Each micro-beamforming cell consists of a pipeline-operated S/H delay line and a V/I converter (Fig. 5.5) and is capable of providing delays from 40 ns to 280 ns, with a step size of 40 ns. The delay time is user-programmable with the three digital inputs $D_0$~$D_2$. The delayed voltage signals are converted into currents by a V/I converter. By connecting the outputs of several beamforming cells, signal summation can thus be easily achieved in the current domain. To mitigate the effects of clock-feed-through and charge injection in the switches, a differential structure is used.

The circuit implementation of the pipeline-operated S/H delay line and the required clock pattern are depicted in Fig. 5.6. To realize the 40 ns delay step size, a sampling frequency of 25 MHz has been chosen. Since the ultrasound signal in this design has a center frequency of 6 MHz and 50% bandwidth, the chosen sampling frequency fulfills the Nyquist criterion, so that the signal information can be recovered from samples. To achieve the 280 ns delay range, 8 pairs of capacitors are needed. Proper sizing of the sampling capacitors is required to keep $kT/C$ noise low. As analyzed in Section 5.4.2, the use of 250 fF sampling capacitors would ensure a $kT/C$ noise voltage of less than 200 $\mu V_{rms}$. Moreover, in every signal path, a source follower is inserted between the sampling capacitor and the output switch to buffer the signal and to isolate the sampling capacitor from the output. This prevents charge re-distribution between the sampling capacitor and parasitic output capacitors, causing fluctuation of the output voltage. However, the addition of source followers increases the power consumption. In this design, the main transistor in each source follower is biased in strong inversion with a biasing current of 1 μA. There are in total 16 source followers which consume about 53 μW from the 3.3 V supply.

Figure 5.7 shows a diagram of the digital circuitry that is capable of generating the clock pattern shown in Fig. 5.6. It consists of two counters. The first counter provides the clock signals for the input sampling switches ($\phi_1$ to $\phi_8$). Meanwhile, the second counter controls the clock signals for the output switches ($\phi_{1d}$ to $\phi_{8d}$). A comparator determines when the three outputs

of the first counter equal the digital inputs $D_0$~$D_2$. Only when this happens will the second counter start counting. In this way, two groups of clock signals with a programmable relative delay are generated.

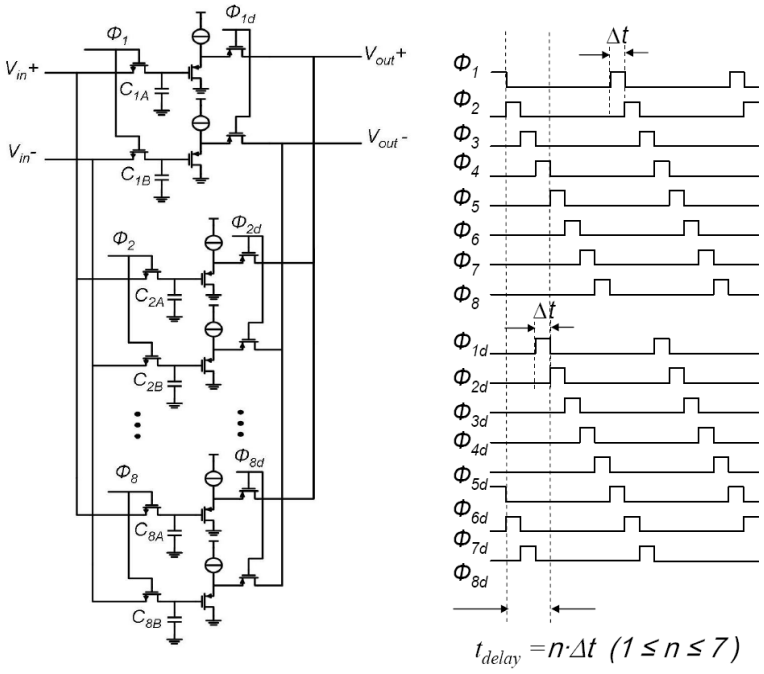



Fig. 5.6 Circuit diagram of the pipeline-operated S/H delay line and the control clocks.

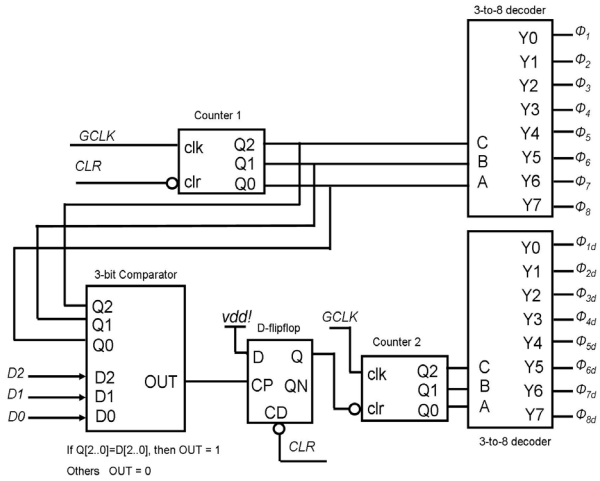



Fig. 5.7 Diagram of the control clock generator.

The V/I converter is implemented based on Caprio's Quad [5.22] (Fig. 5.8). The cross-coupled configuration of this circuit allows it to reproduce the differential input voltage accurately across a resistor $R$, resulting in a current $i$, that is, ideally, independent of the transconductance of transistors $M_1$ to $M_4$:

$$i = (V_{in+} - V_{in-})/R \qquad (5.11)$$

The total DC biasing current of the V/I converter is 8 μA, which results in a power consumption of 26.4 μW from the 3.3 V supply.

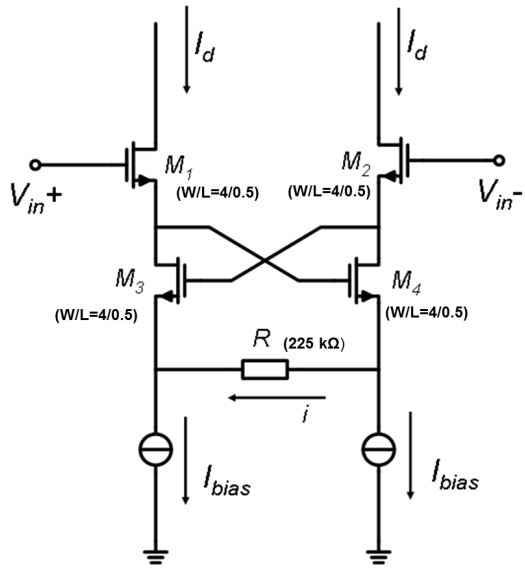



Fig. 5.8 The voltage-to-current (V/I) converter.

## *Measurement Results*

A prototype chip of the micro-beamforming cell has been fabricated in a standard 0.35µm CMOS technology. Figure 5.9 shows a die micrograph, along with a picture of the circuit layout, which is not visible in the micrograph due to the metal coverage. The core area is 0.073 $mm^2$ and the power consumption is 480 µW (25% static and 75% dynamic) for a 25 MHz sampling frequency.

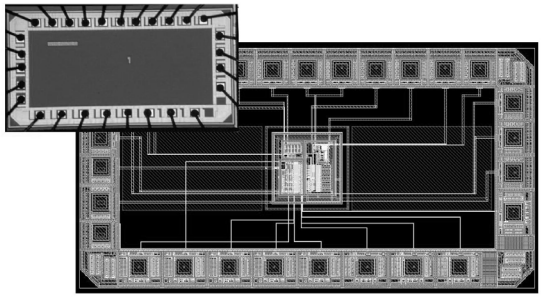


Fig. 5.9 Die micrograph and layout of prototype I.

Figure 5.10 shows the measured output signal of the pipeline-operated S/H delay line for a 6 MHz sinusoidal input pulse and the 7 different delay settings. These results were obtained using a digital oscilloscope. Digital averaging is applied in the oscilloscope so that the delay times can be measured accurately. The initial delay time is 48 ns and the total achievable delay time is 288 ns. The delay step size between any neighboring settings is 40 ns. It can also be observed that the signal amplitude does not change under different delay settings.

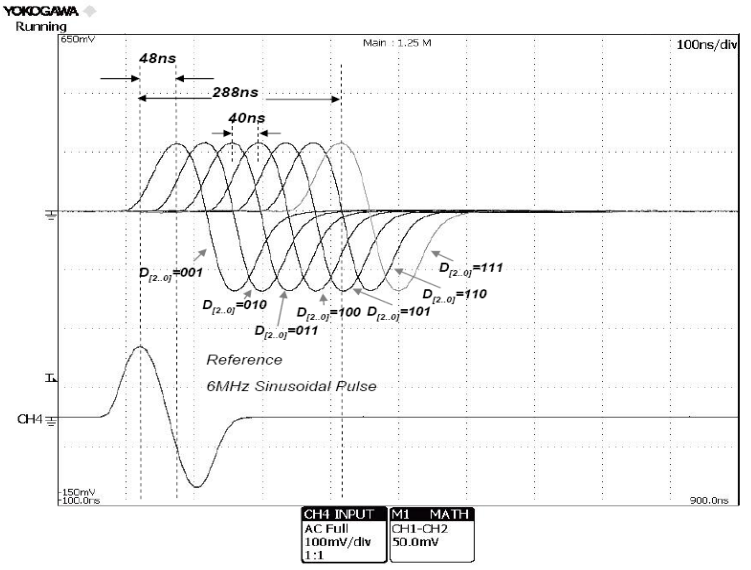



Fig. 5.10 Measured output waveforms for different delay settings.

Figure 5.11 shows the measured gains of 10 samples of the delay line under 7 different delay settings. The measured gains of each sample are normalized to the mean value. It can be seen from the figure that the chip-to-chip gain variation is less than ±0.15 dB for all delay settings, which is negligible compared to the sensitivity variation of the transducer elements.

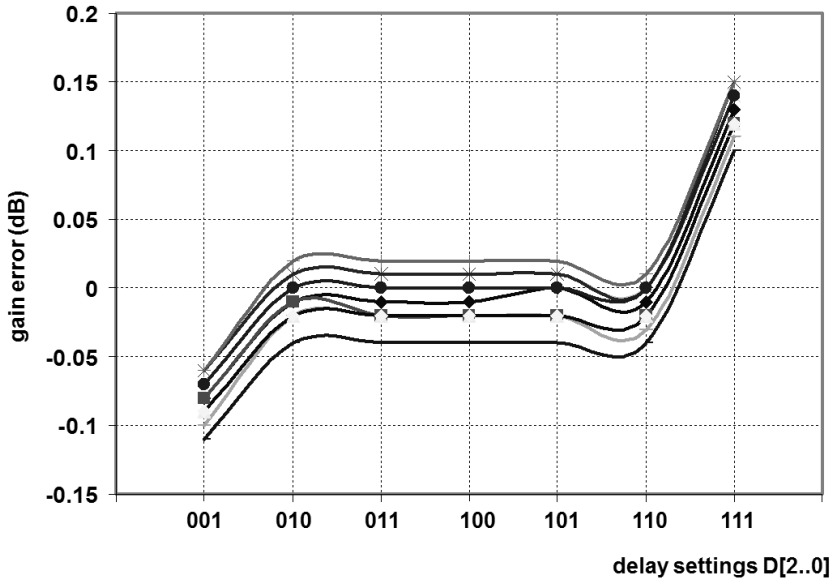



Fig. 5.11 Measured gains of 10 samples of prototype I under 7 different delay settings.

To test the signal dynamic range of the micro-beamforming cell, sinusoidal voltages with a frequency of 6 MHz and amplitudes from about 1 $mV_{p-p}$ to 1 $V_{p-p}$ have been applied to the inputs of the circuit (Fig. 5.5). For ease of measurement, the output differential current is converted into the voltage domain by a trans-resistance amplifier. The output differential voltage of the trans-resistance amplifier versus the input test voltages (Log-Log scale) is plotted in Fig. 5.12. It can be seen that the micro-beamforming cell is able to accommodate input signals with a dynamic range of more than 60 dB, with a gain non-linearity error of less than +/-0.5 dB.

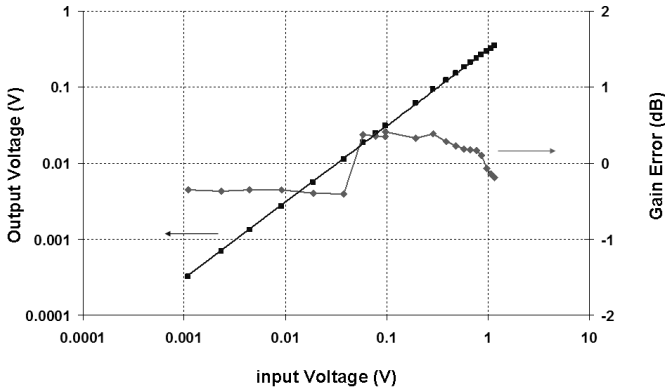



Fig. 5.12 Input signal dynamic range measurement of the micro-beamforming cell (input voltage: 6 MHz sinusoidal signals from about 1 $mV_{pp}$ to $1V_{pp}$) and gain errors in dB (deviation of the measured gain from the value obtained by curve fitting).

### 5.4.4 Prototype II: A 9-Channel Analog Micro-Beamformer with Pipeline-Operated S/H Stages and Charge-Mode Summation

***Circuit Implementation***

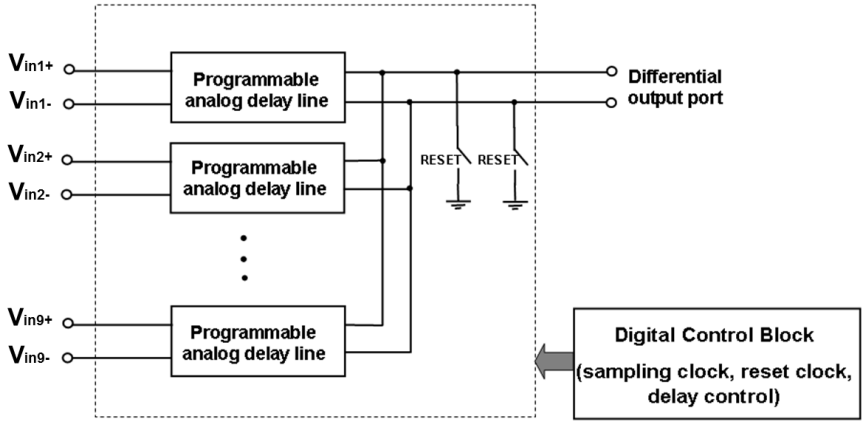



Fig. 5.13 Block diagram of prototype II.

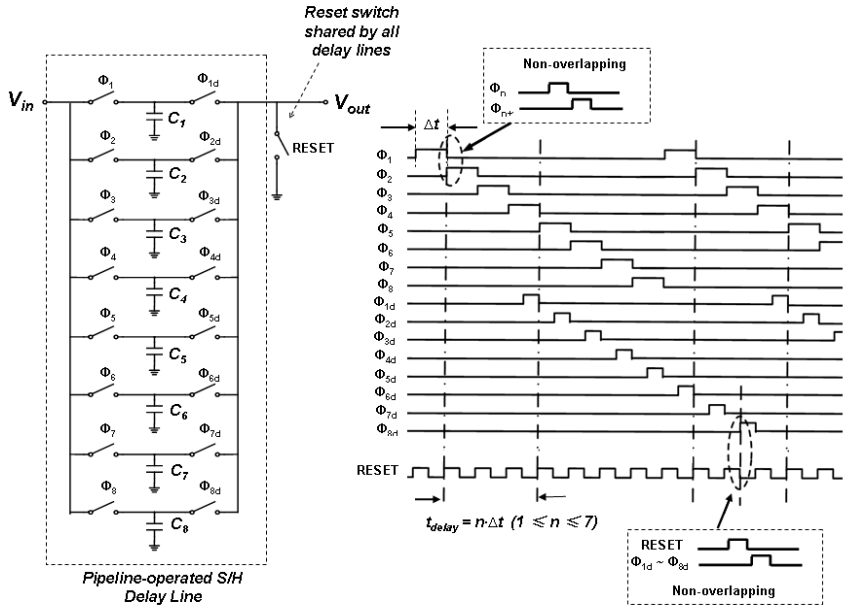



Fig. 5.14 Circuit diagram and clock pattern of one pipeline-operated S/H delay line (only half of the differential signal path is shown).

As shown in Fig. 5.13, the proposed micro-beamformer [5.19] consists of 9 pipeline-operated S/H delay lines and a digital control block. Figure 5.14 shows the circuit diagram and the clock patterns of one of the delay lines, which contains 8 S/H stages (only half of the differential signal path is shown). For a sampling frequency of 25 MHz, the circuit is capable of delaying a signal from 40 ns to 280 ns. The summation is realized by simply routing the outputs of all 9 delay lines together (Fig. 5.14). The resulting charge redistribution among the capacitors of the delay lines effectively averages the delayed signals, which is equivalent to adding and attenuating them. Compared to the voltage-mode summation method [5.15][5.16], this charge-mode approach eliminates the summing amplifier. While compared to the current-summation method [5.12], no extra circuit is required for signal conversion, since the voltage-to-charge conversion is naturally realized in the S/H stage itself. Thus the charge-mode summation method combined with the pipeline-operated S/H delay structure intrinsically leads to circuits with low complexity and high power efficiency. One disadvantage

of the charge-mode summation approach is that there is no signal amplification in the voltage domain. Under the ideal conditions, the voltage gain is unity. However, any parasitic capacitance at the summing node would cause the voltage gain to drop below unity, and thus result in a smaller output voltage signal. This, in turn, requires a lower input noise level for the electronics that processes signals from the output of the micro-beamformer.

For the practical circuit implementation, several design considerations apply. A differential structure and proper sizing of the sampling capacitors are required. A careful layout should be drawn to ensure capacitor matching and to minimize parasitic capacitors on the summing node. To eliminate errors due to residual charge on these parasitic capacitors, a RESET switch is applied to remove this charge before summation (Fig. 5.13 and Fig. 5.14). Finally, non-overlapping clocks are used to avoid unwanted charge distribution and to ensure accurate signal sampling and summation (see the clock diagram in Fig. 5.14). All the edges of clocks $\phi_1$ to $\phi_8$ are non-overlapping, since a sample must be frozen on the capacitor before the next sample can be taken. Besides, the falling edge of the RESET clock and the rising edges of clocks $\phi_{1d}$ to $\phi_{8d}$ must be non-overlapping as well, so that the RESET switch is completely off before the charge-averaging operation occurs. Moreover, a proper shielding scheme is required for the layout, in order to minimize the clock-to-signal coupling and channel-to-channel crosstalk.

Figure 5.15 depicts the block diagram of the digital circuitry that is capable of generating clock patterns for the micro-beamformer. It consists of a 3-bit binary counter, two non-overlapping clock generators, nine 3-bit adders, ten 3-to-8 decoders and some logic gates. The counter together with a decoder and a non-overlapping clock generator provide the non-overlapping clocks $\phi_1$ to $\phi_8$. Meanwhile, there are 9 groups of 3-bit digital inputs which are added to the outputs of the counter by digital adders to provide offsets. These inputs are provided by an on-chip shift register, which allows the offsets to be programmed via a serial interface. The outputs of the adders are further processed by decoders and logic gates to generate clock patterns $\phi_{1d}$ to $\phi_{8d}$ for each delay path. In this implementation, digital adders are used to

achieve relative digital delays. Compared to the implementation shown in Fig. 5.7, where a comparator and an extra counter are employed, the approach shown in Fig. 5.15 is more power efficient. The RESET clock is synchronized with the input clock of the counter. To ensure that the falling edge of the RESET clock and the rising edges of clocks $\phi_{1d}$ to $\phi_{8d}$ are non-overlapping, an extra non-overlapping clock generator is used to generate RESET and $\overline{\text{RESET}}$, which are non-overlapping. The rising edges of clocks $\phi_{1d}$ to $\phi_{8d}$ are synchronized with the $\overline{\text{RESET}}$ signal and therefore are non-overlapping with the RESET signal.

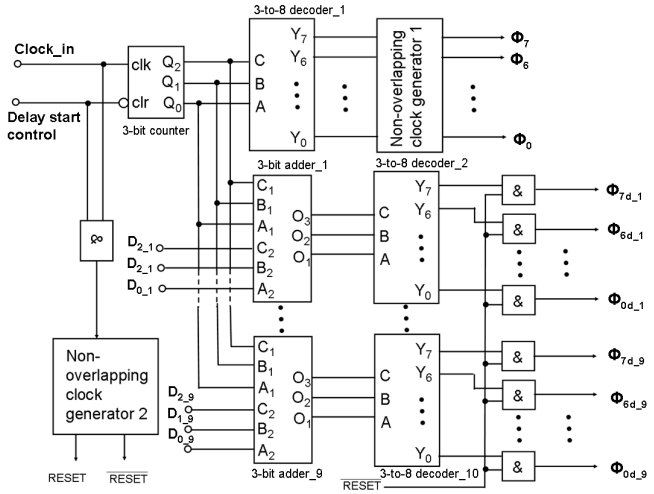



Fig. 5.15 Digital circuitry for prototype II.

### *Measurement Results*

The prototype chip has been fabricated in a standard 0.35 μm CMOS technology. A die micrograph along with a picture of the circuit layout is shown in Fig. 5.16. The core area is 0.25 $mm^2$.

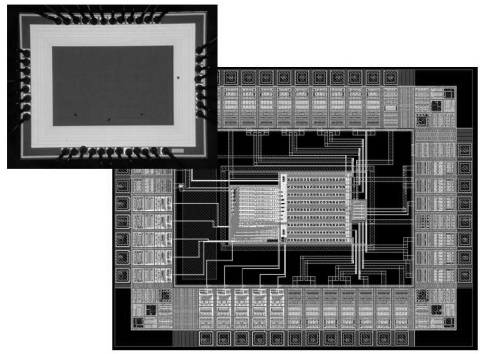


Fig. 5.16 Die micrograph and layout of prototype II.

Figure 5.17a shows the measured output signal of the prototype for the 7 possible delay settings when a 6 MHz sinusoidal input pulse is applied to all channels. The results were obtained using a digital oscilloscope with digital averaging applied. It can be observed that the measured delay step sizes and the total delay range are in agreement with the design targets. Furthermore, the signal amplitude does not change for different delay settings. Figure 5.17b shows the measured output when a 6 MHz sinusoidal pulse is applied to one or more of the delay lines, demonstrating the summing function of the prototype. To estimate the channel-to-channel mismatch, output signals for every channel for different delay settings have been analyzed and plotted in Fig. 5.18. It can be seen from the figure that the channel-to-channel gain variation is less than ±0.3 dB for all the delay settings, which fulfills the design requirement. The micro-beamformer prototype is able to handle a 60 dB input-signal dynamic range (1 $mV_{p\text{-}p}$ to 1 $V_{p\text{-}p}$). The worst-case[1] power consumption is 2.4 mW at a 25 MHz sampling frequency.

[1] The switching rate of the digital circuit differs for delay configurations. The worst-case power consumption is measured for the case that the switching rate is the highest.

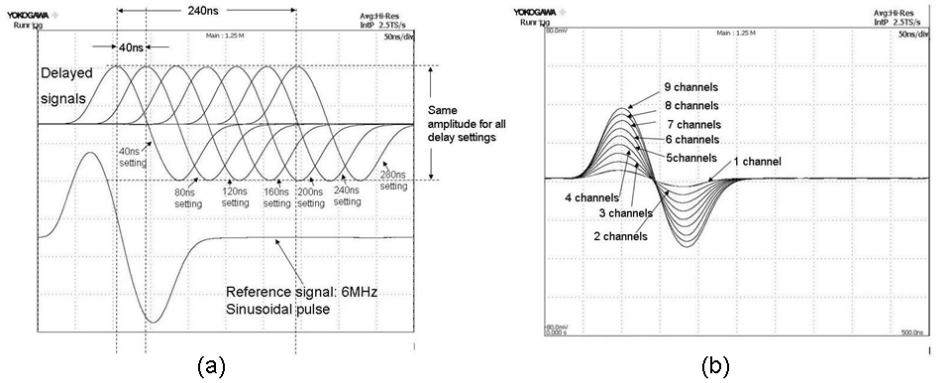



Fig. 5.17 Measured delay-and-sum function: (a) output waveform for different delay settings when all 9 channels have the same delay (sampling rate 25 MHz), and (b) output waveform as a function of the number of input channels to which a signal is applied.

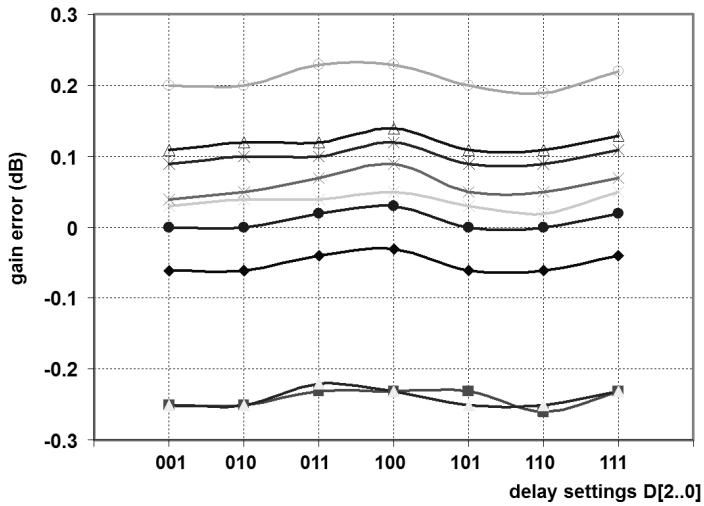



Fig. 5.18 Measured gains of 9 channels for 7 different delay settings of 1 chip.

### 5.4.5 Performance Comparison

TABLE 5.4 PERFORMANCE COMPARISON TABLE.

| Items \ Designs | [5.12] | [5.6] | Prototype I | Prototype II |
|---|---|---|---|---|
| Delay Principle | pipelined sampled delay | all-pass filter type delay | pipelined sampled delay | pipelined sampled delay |
| Summation Principle | current mode | current mode | current mode | charge mode |
| Results based on: | Measurement | simulation | measurement | measurement |
| Technology | 0.8 µm CMOS | 60 GHz Si-Ge BiCMOS | 0.35µm CMOS | 0.35 µm CMOS |
| Supply Voltage | 5V | 2.5 V | 3.3 V | 3.3 V |
| Number of Channels | 16 | 4 | 1 | 9 |
| Number of Delay Cells per Channel | 72 | 4 | 8 | 8 |
| Chip Area | 72 $mm^2$ | information not available | 0.073 $mm^2$ core area | 0.25 $mm^2$ core area |
| Sampling frequency ($f_s$) | 64 MHz | not applicable | 25 MHz | 25 MHz |
| Delay Step Size | 15.6 ns | 57.3 ns at 3 MHz | 40 ns | 40 ns |
| Dynamic Range | 60 dB | < 60 dB | > 60 dB | > 60 dB |
| Total Power Consumption | 1.12 W | 3.2 mW | 480 µW (25% static, 75% dynamic) | 2.4 mW (100% dynamic) |
| Power Consumption per Delay Cell ($P_{cell}$) | 1 mW | 200 µW | 60 µW | 33 µW |
| $P_{cell}/f_s$ (µW/MHz) | 15.625 | not applicable | 2.4 | 1.333 |
| Gain Variations | information not available | information not available | ±0.15 dB (10 samples) | ±0.5 dB (9 channels in 1 sample) |

Measurement results of prototypes I and II confirm that both designs deliver the desired functionality. Their performances are summarized and compared to prior designs[1] [5.6] and [5.12] in Table 5.4. Two important observations are listed below:

- Prototype II offers better power efficiency compared to prototype I. This is thanks to the charge-mode summation method, which eliminates the V/I converters. Power consumption for both prototypes I and II is dominated by digital circuitry.

[1] The prior designs showed in this table are not 100% comparable to prototypes I and II.

- In prototype II, because of the charge-mode operation, errors caused by capacitor mismatches and parasitic capacitances are more crucial than that in prototype I. This results in a higher channel-to-channel gain variation. However, according to the measurement result, the gain variation of prototype II is still less than ±0.5 dB, which fulfills the design requirement.

## 5.5 Conclusions

This chapter has presented the design choices and circuit implementation of the micro-beamforming block in the front-end signal processing chain for 3D TEE. We have chosen to implement micro-beamformers in the analog domain for better power efficiency. The pipeline-operated S/H delay-line structure has been used to realize delays. Design aspects that limit the precision of the S/H delay-line have been explored, such as: residual charge injection, clock feed-through error and *kT/C* noise. It can be concluded that the residual charge-injection error is the dominant error source. Considerations for layout design are briefly discussed. Furthermore, signal-summation methods in the current domain and in the charge domain have been investigated. Two prototype chips have been built for performance evaluation. Measurement results show that the chosen delay structure offers good performance in terms of power consumption, timing accuracy, gain accuracy and flexibility. The prototype chip with the charge-mode summation method shows even better power efficiency compared to the prototype chip with current-mode summation.

## 5.6 References

[5.1] P. Errico, A. Hill, "Choosing high-speed signal processing components for ultrasound systems", *Analog Dialogue*, vol. 29, no. 2, 1995. Available at: http://www.analog.com/library/analogDialogue/archives/29-2/chsnghspeed.html. (January 2012)

[5.2] AD9278 Low-power, octal receiver with CW I/Q demodulator for portable ultrasound, Analog Devices Datasheet. Available at:

http://www.analog.com/static/imported-files/data_sheets/AD9278.pdf. (January 2012)

[5.3] LM96511 Ultrasound receive analog front end, National Semiconductor Datasheet. Available at: http://www.national.com/pf/LM/LM96511.html#Overview. (January 2012)

[5.4] AFE5808 Fully Integrated 8-Channel Ultrasound Analog Front End with Passive CW Mixer for Ultrasound, Texas Instruments Datasheet. Available at: http://www.ti.com/product/afe5808. (January 2012)

[5.5] V. S. Gierenz, R. Schwann, T. G. Noll, "A low power digital beamformer for handheld ultrasound systems", *Proceedings of the 27th European Solid-State Circuits Conference*, Villach, Austria, 2001, pp. 261-264.

[5.6] T. Halvorsrod, W. Luzi, T. S. Lande, "A log-domain μbeamformer for medical ultrasound imaging systems", *IEEE Transaction on Circuits and Systems-I*, vol. 52, no. 12, Dec. 2005.

[5.7] J. R. Talman, S. L. Garverick and G. R. Lockwood, "Integrated circuit beamformer for high frequency array", *Proceedings IEEE Ultrasonics Symposium,* 1999, pp. 1235-1238.

[5.8] J. R. Talman, S. L. Garverick and G. R. Lockwood, "Integrated circuit for high-frequency ultrasound annular array", *Proceedings IEEE Custom Integrated Circuits Conference*, 2003, pp. 447-480.

[5.9] G. Gurun, A. Sisman, J. Zahorian, S. Satir, M. Karaman, P. Hasler, L. Degertekin, "A tunnable analog delay element for high-frequency dynamic beamforming", *Proceedings IEEE International Ultrasonics Symposium*, 2009, pp. 345-348.

[5.10] Y. Mo, T. Tanaka, S. Arita, A. Tsuchitani, K. Inoue, K. Yamashita, Y. Suzuki, "Integrated analog beam former based on bucket brigade device for micromachined ultrasonic sensor array", *Sensors and Actuators A*, vol. 101, no. 1, pp. 203-211, 2003.

[5.11] Y. Mo, T. Tanaka, S. Arita, A. Tsuchitani, K. Inoue, Y. Suzuki, "Pipelined delay-Sum architecture based on bucket-brigade devices for on-

chip ultrasound beamforming", *IEEE Journal of Solid-State Circuits*, vol. 38, no. 10, pp. 1754-1757, 2003.

[5.12] B. Stefanelli, I. O'Connor, L. Quiquerez, A. Kaiser, D. Billet, "An analog beam-forming circuit for ultrasound imaging using switched-current delay lines", *IEEE Journal of Solid-State Circuits*, vol. 35, no. 2, pp. 202-211, 2000.

[5.13] A. Williams, F. Taylor, *Electronic Filter Design Handbook*, 4th Ed., New York: McGraw-Hill, 2006.

[5.14] M. F. Tompsett and E. J. Zimany, Jr., "Use of charge-coupled devices for delaying analog signals*", IEEE Journal of Solid-State Circuits*, vol. 8, no. 2, pp. 151-157, 1973.

[5.15] T. K. Song, J. F. Greenleaf, "Novel ultrasonic dynamic focusing system with reduced hardware complexity", *Proceeding SPIE*, vol. 1733, pp. 141-153, 1992.

[5.16] T. K. Song, J. F. Greenleaf, "Ultrasonic dynamic focusing using an analog FIFO and asynchronous sampling", *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control*, vol. 41, no. 3, pp. 326-332, 1994.

[5.17] B. Savord, R. Solomon, "Fully sampled matrix transducer for real time 3D ultrasonic imaging", *Proceedings IEEE Ultrasonics Symposium*, 2003, pp. 945-953.

[5.18] D. Zhao, W. A. Serdijn, "A time-interleaved sampling delay circuit for IR UWB receivers", *Proceedings IEEE International Symposium on Circuits and Systems*, 2009, pp. 233-236.

[5.19] Z. Yu, M. A. P. Pertijs, G. C. M. Meijer, "Ultrasound beamformer using pipeline-operated S/H delay stages and charge-mode summation", *Electronics Letters*, vol. 47, issue. 18, pp. 1011-1012, 2011.

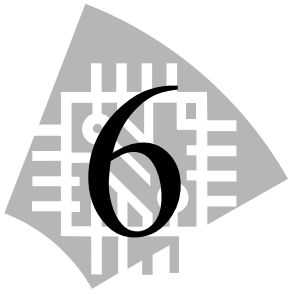
[5.20] B. Razavi, *Design of Analog CMOS Integrated Circuits*, Boston: McGraw-Hill, 2001.

[5.21] Z. Yu, M. A. P. Pertijs, G. C. M. Meijer, "A programmable analog delay line for micro-beamforming in a transesophageal ultrasound probe",

*Proceedings IEEE International Conference on Solid-State and Integrated Circuit Technology*, 2010, pp. 299-301.

[5.22] R. Caprio, "Precision Differential Voltage-current Converter", *Electronics Letters*, vol. 9, no. 6, pp. 147-148, Mar. 1973.

# *Ultrasound Receiver Realizations*




In the previous chapters, the designs of the key building blocks of the front-end receive signal processing chain for 3D TEE, i.e. an LNA, a time-gain-compensation (TGC) amplifier, and micro-beamforming circuitry, have been elaborated. In this chapter, we present two ultrasound receivers, which were designed using the aforementioned building blocks. The first design is a 3-channel receiver implemented on a PCB (Section 6.1) [6.1]. Measurement results of this receiver confirm the effective functionality of the signal-processing chain. Based on the promising results obtained with the PCB demonstrator, a 9-channel receiver ASIC has been designed and fabricated (Section 6.2). This 9-channel receiver chip has been used to readout 3×3 Rx transducer elements. Measurements show that the ASIC is capable of processing real ultrasound signals. The arrangements of two receiver designs are summarized in terms of building blocks in Table 6.1.

TABLE 6.1 BUILDING BLOCKS IN THE TWO ULTRASOUND RECEIVER DESIGNS

| Building Blocks | Number of building blocks involved | |
|---|---|---|
| | Design I (PCB implementation of a 3-channel ultrasound receiver) | Design II (An integrated 9-channel ultrasound receiver ASIC) |
| LNA (Section 4.2) | None | 9 |
| TGC amplifier (Section 4.3) | 3 | 9 |
| Micro-beamforming cell with pipeline-operated S/H delay line and a V/I converter (Section 5.4.3) | 3 | None |
| A 9-channel analog micro-beamformer with pipeline-operated S/H stages and charge-mode summation (Section 5.4.4) | None | 1 |

## 6.1 PCB Implementation of a 3-Channel Ultrasound Receiver

### 6.1.1 System Description

Figure 6.1 shows the block diagram of the receiver PCB. It consists of three prototype TGC-amplifier ICs, three micro-beamforming cells, and some peripheral circuits. The prototype ICs are assembled using chip-to-PCB bonding, as shown in Fig. 6.2. We use this ultrasound receiver PCB to experimentally evaluate the performance of the signal-processing chain and to establish the main characteristics of the ICs and the system, such as the programmable delay time, the summation function, and the power dissipation.

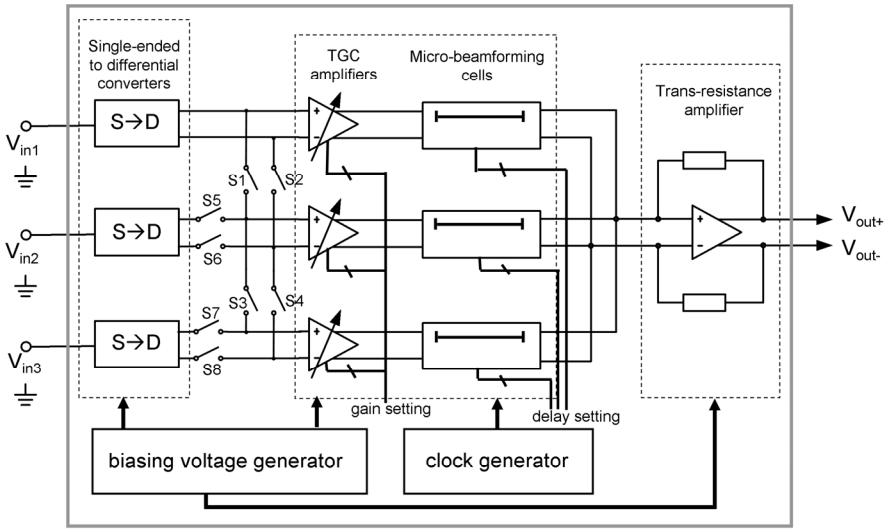



Fig. 6.1 Block diagram of the ultrasound receiver PCB

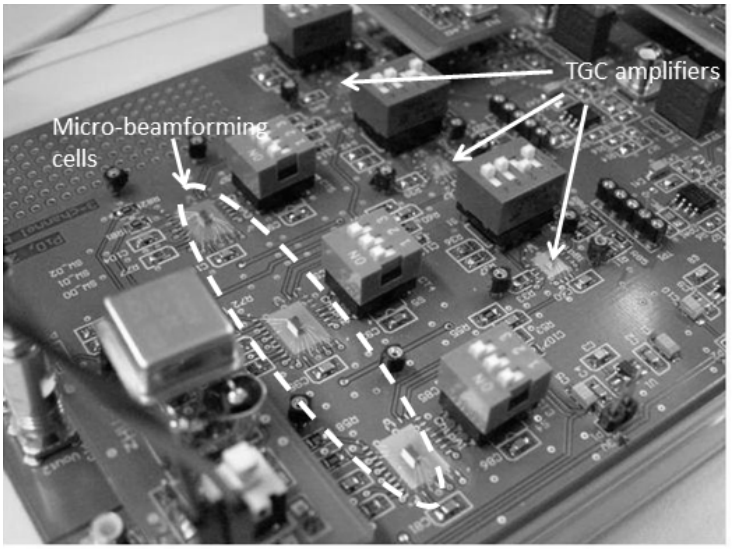



Fig. 6.2 Photograph of the PCB (prototype ICs are assembled using chip-to-PCB bonding).

The 3-channel ultrasound receiver PCB has three single-ended inputs and one differential output. The single-ended input signals are converted into differential signals via on-board single-ended to differential converters. For

testing purposes, by controlling switches $S_1$ to $S_8$, the following TGC amplifiers and micro-beamforming cells can be configured to process either the same input signal together, or a dedicated input signal individually. A gain of 0 dB, 12 dB, 26 dB or 40 dB can be chosen for each TGC amplifier by on-board ON/OFF switches. Each micro-beamforming cell can have seven different delay settings from 40 ns to 280 ns, with a step size of 40 ns, which can be selected by generating appropriated voltage levels on the PCB board and then feeding them into the digital input ports of the micro-beamforming cell. As described in Section 5.4.2, the signals at the output of the micro-beamforming cells are in the form of current. These currents are summed up by routing the outputs of the micro-beamforming cells together and converted into the voltage domain by an on-board trans-resistance amplifier. Additional on-board peripheral circuits are used to provide proper biasing voltages and clocks.

### 6.1.2 Experimental Results

Since the performance of each individual building block has already been evaluated in the previous chapters, we will now focus on testing the overall system functionality. In the first measurement, three Gaussian pulses are applied to the three inputs of the receiver PCB. These signals are centered at 6 MHz, with a 50% bandwidth. As shown in Fig. 6.3, the relative delays between the signals are 200 ns and 120 ns. By programming the delay settings for each channel (delay codes: 110, 100 and 001 for channel 1 to 3), and having the sampling clock running at 25 MHz, the three input signals are delayed by 240 ns, 160 ns and 40 ns, respectively. As can be seen from Fig. 6.3, this aligns the signals in time, resulting in a single output pulse.

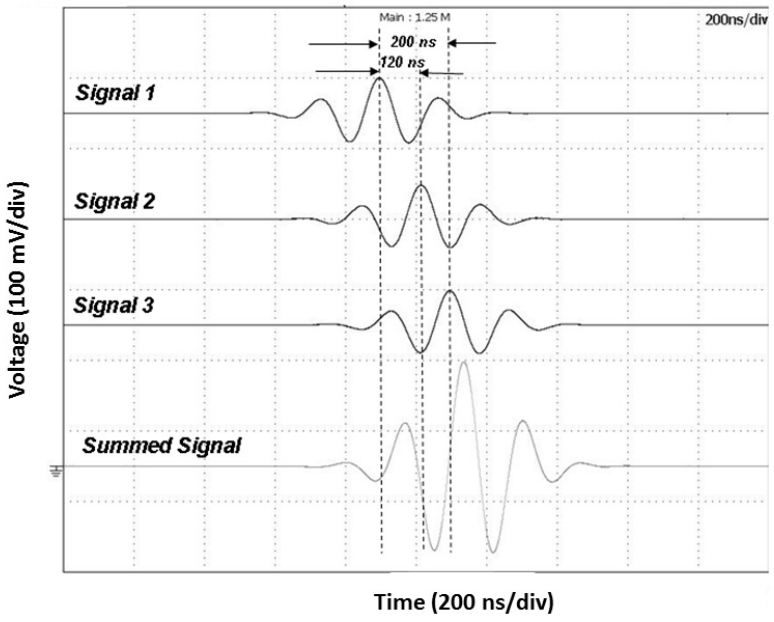



Fig. 6.3 Measurement of the micro-beamforming function: three Gaussian input pulses are applied, centered at 6 MHz, with a 50% bandwidth, and with relative delays of 200 ns and 120 ns. The three on-board micro-beamforming cells are programmed to have different delays (240 ns, 160 ns and 40 ns for signal 1, signal 2 and signal 3) to sum up the signals coherently.

In the second measurement, all three TGC amplifiers are set to have the same gain and receive the same Gaussian-shaped sine wave with center frequency of 6 MHz and a 50% bandwidth from the input port $V_{in1.}$ All three micro-beamforming cells are set to have the same delay time. Figure 6.4 shows the result of a Fast Fourier Transform (FFT) analysis for the signal at the input port and the summed signal at the output port of the PCB, respectively (Fig. 6.1). It can be concluded from the figure that the circuits do not affect the bandwidth or the center frequency of the signals.

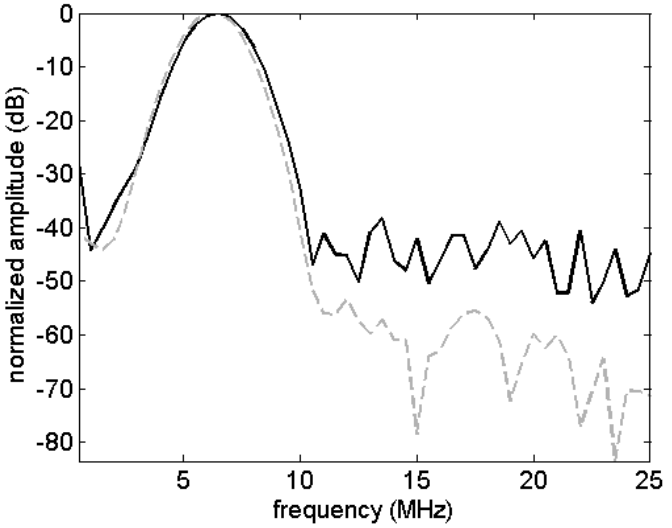



Fig. 6.4 The normalized magnitude of the FFT of the summed output signal (gray dashed) compared to that of the input signal (black solid).

As described in Section 4.2.4 and Section 5.4.3, the measured power consumption of a TGC amplifier and a micro-beamforming cell is 130 µW and 480 µW, respectively. Together with an expected power consumption of about 100 µW for the LNA (Section 4.2), the total power consumption of the receiver electronics per transducer element amounts to about 0.7 mW. When we scale up this value for the whole matrix transducer with about 2000 elements, the total power consumption is around 1.4 W, which is in the range of the design requirement described in Chapter 3 (Section 3.3). The 3-channel ultrasound receiver realized on a PCB delivers a proof of concept for the front-end electronics design for an ultrasound matrix transducer.

## 6.2 An Integrated 9-Channel Ultrasound Receiver ASIC

### 6.2.1 System Description

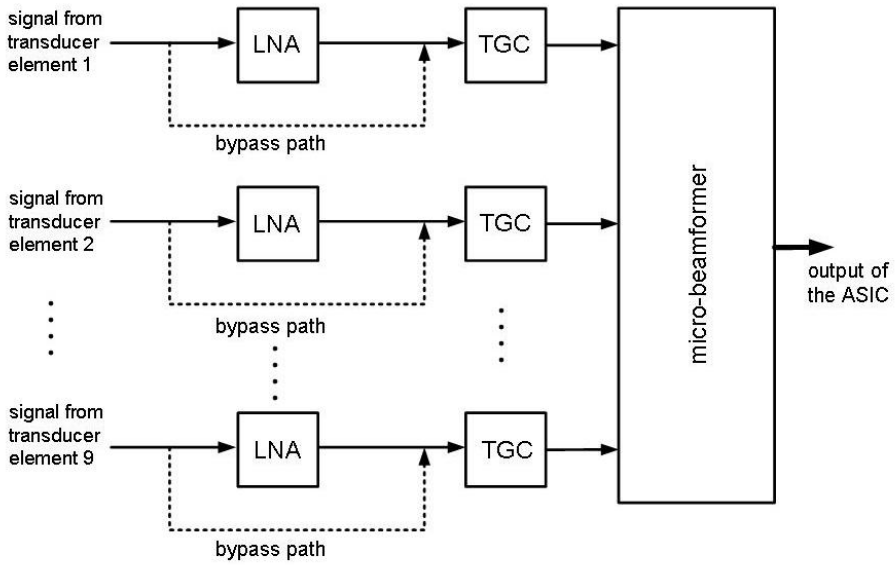



Fig. 6.5 Block diagram of the 9-channel receiver ASIC.

In Fig. 6.5, a block diagram of the 9-channel receiver ASIC is depicted. It is designed to interface a receive-transducer sub-group with 3×3 elements. The main building blocks of the ASIC are the LNAs, TGC amplifiers and a micro-beamformer. The LNA can be bypassed in the case of large input-signal levels (Section 4.1). The TGC amplifier is capable of providing four discrete gains. With the bypass option available for the LNA, there are 8 gain configurations in total for the ASIC, which are summarized in Table 6.2. The basic circuits of the LNA and the TGC amplifier have been described in Chapter 4. However, to enable the bypass option of the LNA, properly connecting of the LNA and TGC is required. The connection scheme of the LNA and TGC will be discussed in the next section. The micro-beamformer is based on the pipeline-operated S/H stages with charge-mode summation [6.2]. We applied the circuit block described in Section 5.4.4.

TABLE 6.2 GAIN CONFIGURATIONS OF THE 9-CHANNEL ULTRASOUND RECEIVER ASIC.

| LNA | TGC | Total gain |
|---|---|---|
| Bypass | 0dB | 0dB |
| Bypass | 12dB | 12dB |
| Bypass | 26dB | 26dB |
| Bypass | 40dB | 40dB |
| 20dB | 0 | 20dB |
| 20dB | 12dB | 32dB |
| 20dB | 26dB | 46dB |
| 20dB | 40dB | 60dB |

## 6.2.2 LNA-TGC Connection Scheme

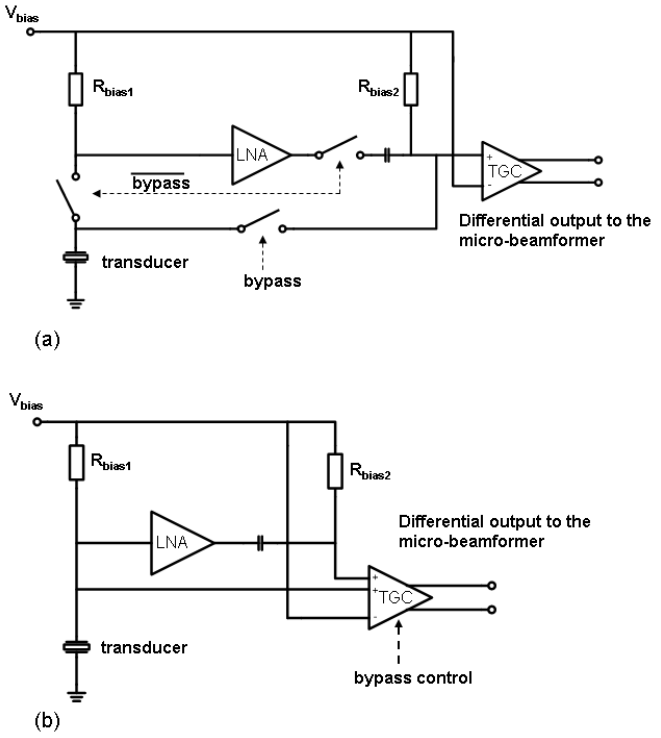



Fig. 6.6 LNA and TGC amplifier connection schemes: (a) using of switches between the transducer output, the LNA and the TGC amplifier (b) using a TGC amplifier with an auxiliary input.

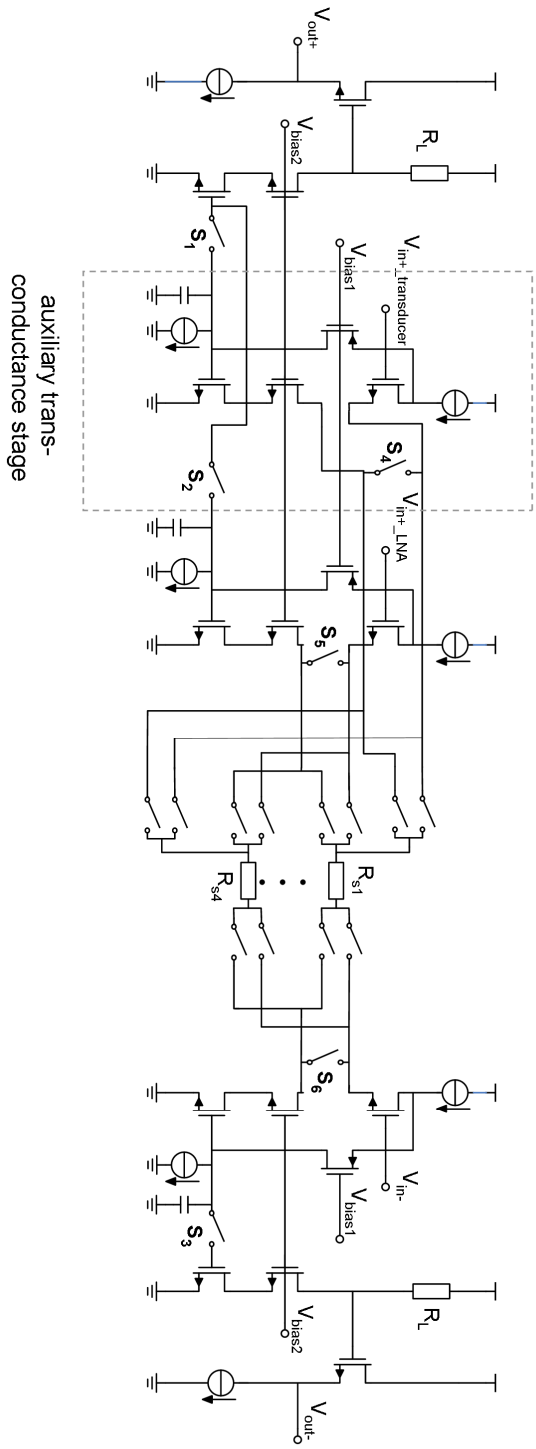



Fig. 6.7 TGC amplifier with an auxiliary input trans-conductance stage.

In our design, the TGC amplifier is operated as a pseudo-differential amplifier which converts the single-ended signal from either the output of the LNA or the transducer output into a differential signal. This differential signal can be fed directly into the micro-beamformer for further signal processing. One straightforward scheme of connecting the LNA to the TGC amplifier with the bypass option available is to add switches between the transducer output, the LNA and the TGC amplifier, as illustrated in Fig. 6.6a. However, in this scenario, the switching action happens directly at the inputs of the amplifiers. Circuit simulation shows that switching spikes are visible in the input signal. Moreover, the switches are implemented using MOSFETs, which suffer from clock feed-through problem. Since the input biasing voltages of the LNA and the TGC amplifier are set via large biasing resistors, the switching spikes and the voltage steps generated due to clock feed-through take relatively long time to die out, which results in disturbances of the input biasing voltages.

To avoid this problem, a new connection scheme has been proposed. As shown in Fig. 6.6b, the TGC amplifier is equipped with an auxiliary input trans-conductance stage. Depending on the setting, the TGC amplifier can select input signals either from the LNA output or directly from the transducer. The schematic of the TGC amplifier with the auxiliary input trans-conductance stage is depicted in Fig. 6.7. To ensure proper operation of the circuit, an extra set of Kelvin switches is added and several control switches are inserted. Switches $S_1$~$S_6$ are used in conjunction with the input selection. Their settings are summarized in Table 6.3. Switches $S_1$ and $S_2$ are operated in a complementary fashion (the same as switches $S_4$ and $S_5$). By controlling switches $S_1$ and $S_2$, we can connect either the main trans-conductance stage or the auxiliary trans-conductance stage to the remaining circuit stages. The function of $S_4$ or $S_5$ is to sustain the normal DC operating point when the corresponding trans-conductance stage is disconnected. Switches $S_3$ and $S_6$ are dummies to maintain the balance of the circuit. Switch $S_3$ is always closed, while, switch $S_4$ is always open. The proposed LNA-TGC connection scheme prevents the switching action from occurring directly at the inputs of the amplifiers. Therefore, the input signals and the input biasing voltages are kept unaltered. However, one disadvantage is the

increased power consumption, since additional power is needed for the auxiliary trans-conductance stage.

TABLE 6.3 SETTINGS OF SWITCHES $S_1$ TO $S_6$ IN THE TGC AMPLIFIER WITH AN AUXILIARY INPUT.

| Input selection | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ |
|---|---|---|---|---|---|---|
| Signal from the LNA's output | open | closed | closed | closed | open | open |
| Signal from the transducer | closed | open | closed | open | closed | open |

### 6.2.3 Experimental Results

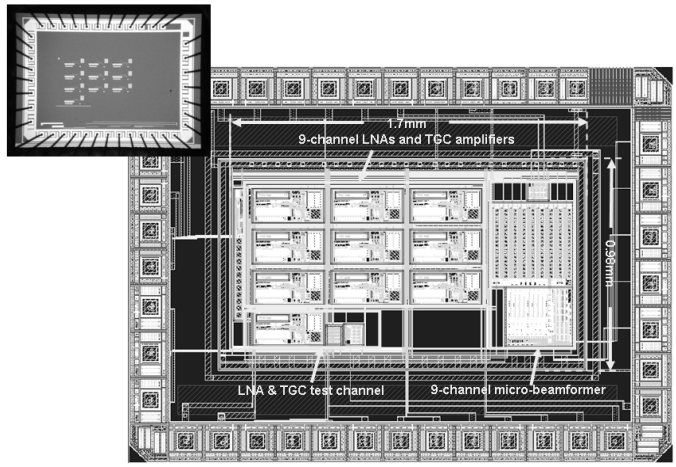



Fig. 6.8 Die micrograph and layout of the 9-channel receiver ASIC.

The receiver ASIC has been implemented in a 0.35 µm CMOS process from ON Semiconductor. The die micrograph and the chip layout are shown in Fig. 6.8. The core area of the chip is 0.98 mm × 1.7 mm, which could be further reduced by optimizing the layout. In order to evaluate the circuit performance, test structures, i.e., an extra test channel with a combined LNA-TGC amplifier and buffer circuits, have been implemented on chip (Fig. 6.8). Layout optimization to allow fabrication for a transducer array on top of the chip is a task for future research work.

The ASIC is operated at a 3.3 V supply for both the analog and digital circuitry. The total power consumption (static plus dynamic) of the ASIC in the worst case[1] is 4.85 mW. The static power consumption is 2.55 mW, which is contributed by 10 LNAs and 10 TGC amplifiers (the power consumption of the test LNA-TGC block is included as well). The dynamic power consumption is 2.3 mW, which is contributed by the 9-channel micro-beamformer. The total power consumption per channel, which includes an LNA, a TGC amplifier and 1/9 of the micro-beamformer, is about 0.5 mW. Compared to the receiver PCB presented in Section 6.1, the power consumption per channel has reduced by 0.2 mW. For TEE applications, it is desirable to further reduce the power consumption. Optimization still can be accomplished based on the current design. Proposals for this will be presented in Chapter 8.

To have an impression of the channel-to-channel mismatch of the complete signal processing chain, a 6 MHz sinusoidal test signal is applied to every input channel separately. During this measurement, every channel gets the same gain (20 dB LNA and 0 dB TGC amplifier) and time delay (80 ns setting). The measured output voltages have a variation within ±1 dB among 9 channels[2].

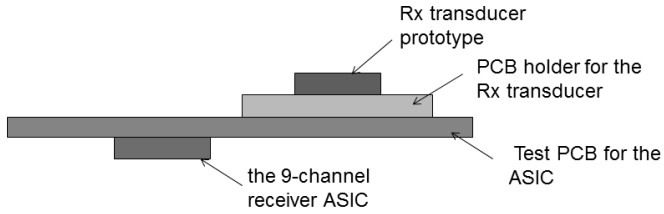



Fig. 6.9 The connection of the prototype ASIC to a Rx transducer prototype via PCBs for measurement.

[1] The switching rate of the digital circuit is different for different delay configurations. The worst-case power consumption is for the case that the switching rate is the highest.

[2] The measured gain variations of LNAs (±1 dB) and TGC amplifiers (±0.5 dB) are chip-to-chip, rather than channel-to-channel. For the prototype 9-channel receiver ASIC, the measured variation is channel-to-channel. Therefore, we expect a smaller gain variation compared to the chip-to-chip case.

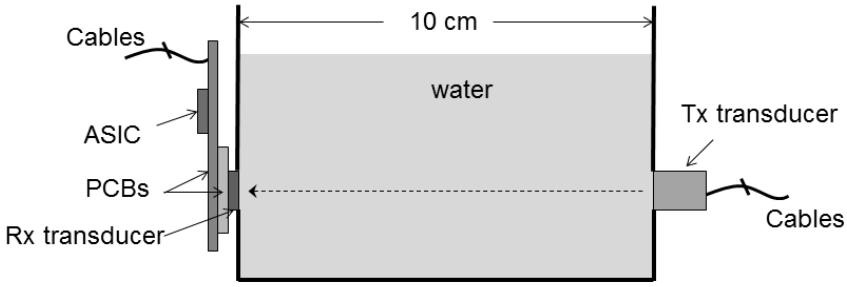



Fig. 6.10 Measurement setup: The ASIC processes the echo signals received from 9 Rx transducer elements. A Tx transducer opposite to the Rx transducer at a distance of 10 cm. Water is the medium for the ultrasound propagation.

In order to test the functionality of the ASIC when processing real ultrasound signals, we connected the ASIC to a receive (Rx) transducer prototype (Chapter 7) via PCBs to read out received signals from 3×3 Rx elements as illustrated in Fig. 6.9. There are two PCBs used to form the connection. The first PCB plays a role as a holder for the Rx transducer prototype. It is connected to one side of the second PCB, on which the ASIC prototype is mounted on the other side. The second PCB also contains some peripheral circuitry (not shown), e.g. voltage regulators, digital buffers, which are used for the ASIC measurement purpose. Figure 6.10 depicts the measurement set up, in which the receive (Rx) transducer together with the ASIC and the PCBs are mounted on the left sidewall of a water tank, while a transmit (Tx) transducer is mounted on the right sidewall of the water tank. The Tx transducer is directly in front of the Rx transducer at a distance of 10 cm. It is driven by the ultrasound pulses from the LeCoeur [6.3] ultrasound machine. Since the surfaces of the Tx and the Rx transducer are in parallel, all Rx elements receive ultrasound signals from the Tx transducer without relative delays. Figure 6.11 shows the signals measured directly at the transducer's electrodes for 9 elements. Figure 6.12 shows the output voltages element-wise corresponding to the locations of the elements in the 3 × 3 group. The results were obtained by an oscilloscope. It can be observed from Fig. 6.11 and Fig. 6.12 that all echo signals are almost aligned in time

with the same shape and small amplitude variations due to unequal sensitivities.

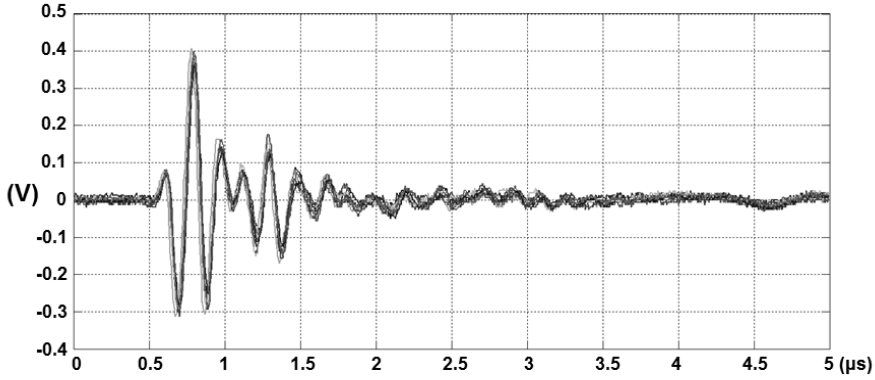



Fig. 6.11 Received ultrasound signals measured at the electrodes of 9 Rx transducer elements.

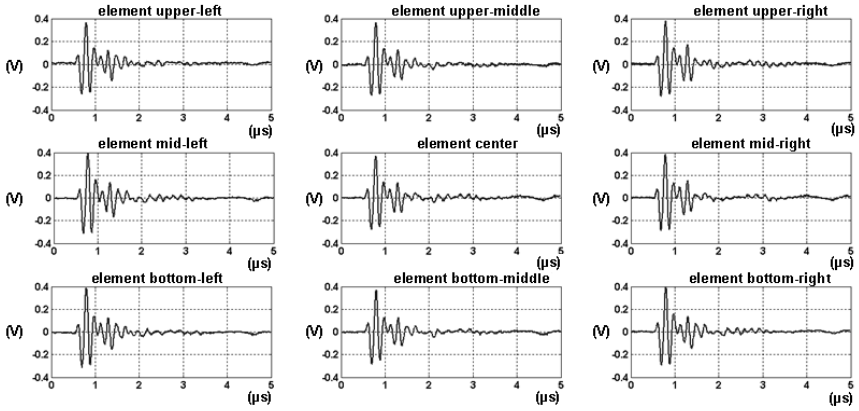



Fig. 6.12 Received ultrasound signals measured at the electrodes of 9 Rx transducer elements (waveforms plotted element-wise with the location of each element indicated).

Next, we applied delays to the micro-beamformer in the ASIC. Since the signal level at the transducer output is already large (Fig. 6.11 and Fig. 6.12), during this measurement, the LNAs are bypassed and all TGC amplifiers get the 0 dB gain setting. Low-pass filtering and averaging functions are applied

in the digital oscilloscope in order to see the acquired signals clearly. Figure 6.13 shows the measured output voltages of the ASIC when uniform delays are applied to all delay lines under three delay configurations. As described in section 5.4.3, the output voltage is the average value of the signals from 9 channels. It can be seen from Fig. 6.13 that the output waveform moves to the right when the delay time is increased from the 40 ns setting to the 200 ns setting in two steps. Each step introduces a delay of 80 ns.

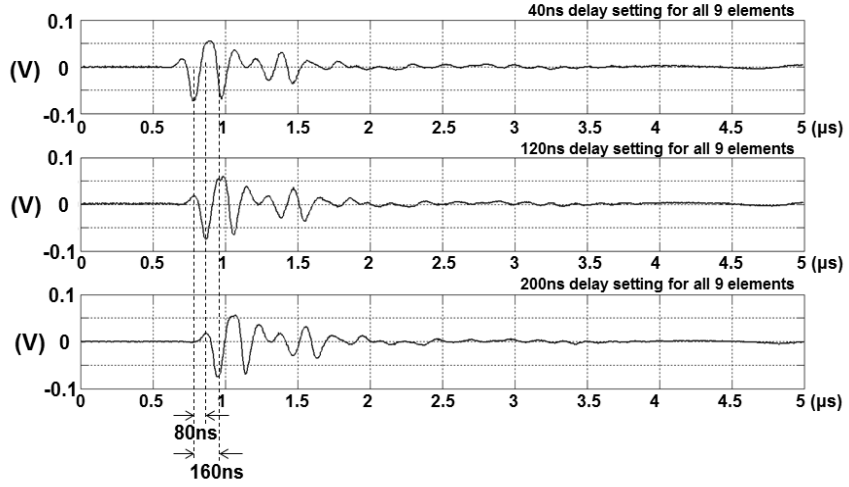



Fig. 6.13 Measured output waveforms for 3 different delay settings (40 ns, 120 ns and 200 ns) when all 9 channels have the same delay.

To further test the beamforming function, we divided the 9 Rx transducer elements into 3 groups and applied 3 different delays (40 ns, 160 ns and 280 ns) to each group. The measured output voltage is depicted in Fig. 6.14 together with a waveform (dashed line) showing the case when all 9 transducer elements get the same delay. It can be seen that by deliberately introducing delays, the echo signals from 9 transducer elements are added out of phase, thus resulting in an output signal with reduced amplitude.

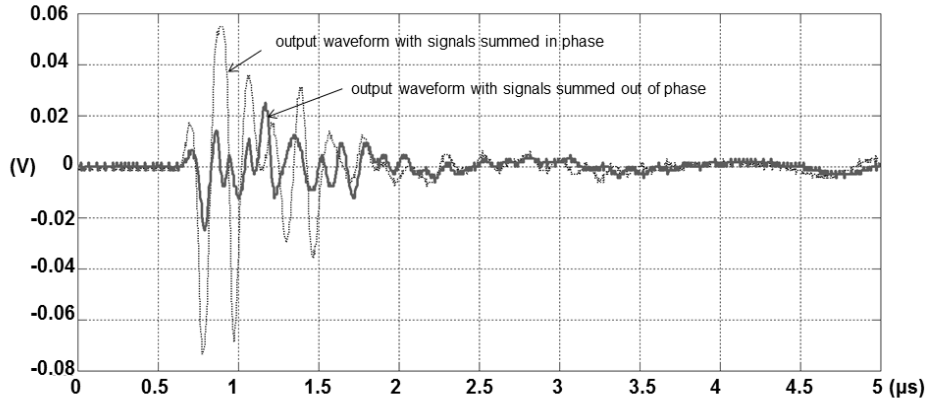



Fig. 6.14 Measured output waveforms with signals summed in phase and out of phase.

The experimental results show that the 9-channel ultrasound receiver ASIC is capable of handling real ultrasound signals. More detailed measurements, e.g. the sensitivity study, distortion, beamforming in different angles, will be carried out in the follow-up research.

## 6.3 Conclusions

This chapter presents the implementation of two front-end ultrasound receivers for application in 3D TEE. The first receiver is implemented on a PCB using prototype ICs for the TGC amplifier and the micro-beamforming cell. The second receiver is a 9-channel ASIC with all required building blocks, i.e., LNAs, TGC amplifiers and a micro-beamformer, integrated on a single chip. Measurement results obtained with both receivers confirm the effectiveness of the signal processing methodology. The design of the second receiver, i.e., the 9-channel ultrasound receiver ASIC, is an important step for the whole project. Our final goal is to design an ASIC which can process echo signals from a matrix Rx transducer with 45 × 45 transducer elements. As described in Section 3.3, the targeted ASIC consists of 225 similar 9-channel sub-circuits in parallel. Now, we have demonstrated that the 9-channel sub-circuit prototype is able to process real ultrasound signals

in a proper way. Based on the promising results, the design approach could be scaled up in the future to accommodate the full transducer array.

## 6.4 References

[6.1] Z. Yu, S. Blaak, Z. Chang, J. Yao, J.G. Bosch, C. Prins, C. T. Lancée, N. de Jong, M. A. P. Pertijs, G. C. M. Meijer, "Front-end receiver electronics for a matrix transducer for 3D transesophageal echocardiography", *IEEE Transaction on Ultrasonics, Ferroelectrics, and Frequency Control*, in press.

[6.2] Z. Yu, M. A. P. Pertijs, G. C. M. Meijer, "An ultrasound beamformer using pipeline-operated S/H delay stages and charge-mode summation," *Electronics Letters*, vol. 47, no. 18, pp. 1011-1012, Sept. 2011.

[6.3] Lecoeur Electronique, http://www.lecoeur-electronique.com/ (January 2012)

# Transducer-to-ASIC Interconnection Method


*The main content in this chapter is patent pending.*

From Chapter 3 to Chapter 6, the front-end receive-signal processing method and the circuit implementation of the receive ASIC for a matrix ultrasound transducer for 3D TEE application have been discussed in depth. In addition to the circuit design, the way of electrically connecting the ASIC to the matrix ultrasound transducer is an important challenge. To tackle the challenge, we −− a team of Oldelft Ultrasound B.V., Electronic Instrumentation Lab of TU Delft and DIMES Technology Center of TU Delft, have successfully developed an interconnection method, which is presented in this chapter. In Section 7.1, the design requirements are described. This is followed by an evaluation of the prior art in Section 7.2. Afterwards, in Section 7.3, the proposed interconnection method is introduced. The effectiveness of the proposed interconnection method is confirmed by a prototype design in Section 7.4. Finally, conclusions are given in Section 7.5.

## 7.1 Design Requirements

In our research, we are exploring an ASIC-to-transducer interconnection scheme that is simple, reliable and compact. The Rx matrix transducer is made of PZT material (CTS 3203HD [7.1]) and consists of 45 × 45 elements. Each element has a surface area of 170 μm × 170 μm and the spacing between adjacent elements is 30 μm. An ASIC is used to read out the signals from the transducer elements. The electrical interconnections between the input channels of the ASIC and the electrodes of the transducer elements must be established. The main design requirements are listed below:

- The whole interconnection structure must fit in the available space in the TEE probe tip (length: 2 cm; width: 1 cm; height: 1 cm).
- The Curie point of the chosen PZT material (CTS 3203HD) is 225°C. As discussed in Chapter 2, to avoid de-polarization of the piezo-material during the interconnection process, the process temperature must be controlled well below 225°C and preferably below 50% of the Curie temperature.
- The interconnection scheme must be reliable and the interconnection structure must not introduce significant parasitic capacitance, resistance, etc.
- The matrix transducer is made by dicing a piece of piezoelectric material in two orthogonal directions to separate the individual elements. Once the elements have been separated, the transducer is no longer mechanically strong. During the interconnection process, mechanical damage to the transducer elements must be avoided. Therefore, the dicing process must be compatible with the interconnection process.

## 7.2 Evaluation of Prior Art

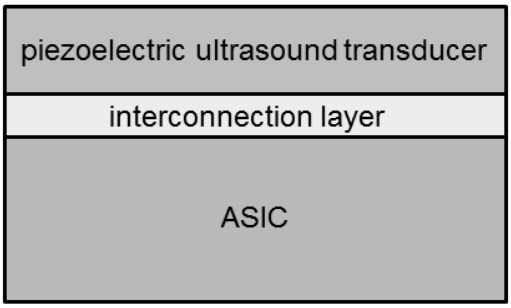



Fig. 7.1 An illustration of a vertical connection scheme between the transducer and the silicon chip.

Since the integration of an ASIC with a piezoelectric transducer for 3D ultrasound imaging is a rather new research topic, there are only a few prior designs reported in the open literature. For example, in [7.2], the interconnection is achieved by using a so-called "interconnection block", where a matrix transducer is attached to one surface of the block and multiple ASICs are connected to the other surfaces of the block. There are metal traces inside the block to form the electrical conduction paths between the ASICs and the matrix transducer. This interconnection block reported in [7.2] has a volume that surpasses the available space for our application. Meanwhile, we believe the most space-saving way to assembly is to have a vertical interconnection, i.e., to stack the ASIC and the Rx transducer (Fig. 7.1). This arrangement also helps to achieve shorter connections for better performance in terms of lower parasitic capacitance, resistance, etc., than can be obtained with the design in [7.2]. It is worth noting that an important advantage of the interconnection method in [7.2] is that the pitch of the transducer elements and the circuits on the ASIC can be different. In contrast, with the vertical interconnection scheme, we must ensure that the sizes of the transducer and the ASIC are compatible.

To achieve a vertical interconnection between the transducer and the ASIC, we naturally thought of the flip-chip technology [7.3]. We investigated whether it would be possible to bond the ASIC directly on top of the matrix transducer using conventional flip-chip technology. However, several practical issues make the flip-chip technology currently not the optimal choice for our specific design. For instance, the PZT material is not a standard substrate material used in flip-chip technology. Moreover, for most solder bump alloys, the melting temperatures are higher than or close to the Curie point of the chosen PZT material (CTS 3203HD).

In [7.4], another vertical interconnection scheme has been investigated by Fuller et al., in which a double-sided flex circuit and a double-layer PCB are used as the intermediate routing vehicles. The ASICs are connected to the front-side of the flex circuit by means of a flip-chip process. A piezoelectric matrix transducer is fixed on the back-side of the PCB. The back-side of the flex circuit is connected to the front-side of the PCB by means of an anisotropic electrically-conducting interface. The advantage of this method is that the ASIC-to-flex circuit and the transducer-to-PCB interconnection processes can be separated. A standard flip-chip technique is suitable for ASIC-to-flex circuit interconnection. Meanwhile, the transducer-to-PCB interconnection process is also a mature technique employed in ultrasound transducer assembly. Furthermore, the use of the anisotropic electrically-conducting interface between the flex circuit and the PCB allows a low temperature process. However, this interconnection method involves complex processing steps. Between the ASIC and the transducer, there are three interfaces, which increases the chance of failure.

## 7.3 Proposed Interconnection Method

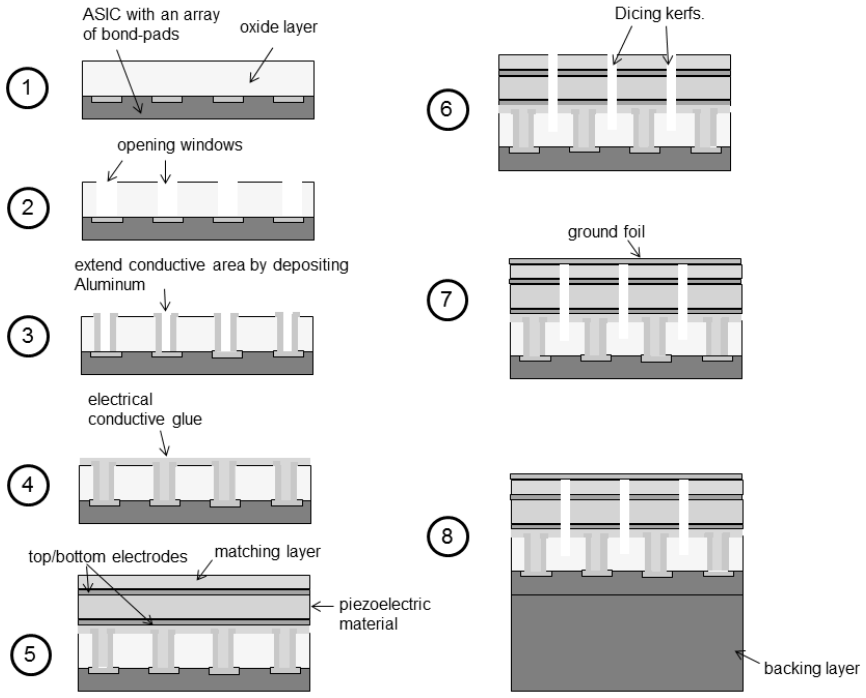



Fig. 7.2 Process flow of the proposed interconnection method (only for illustration purposes, the thicknesses of the layers are not to scale).

The proposed interconnection scheme is depicted in Fig. 7.2. The starting material is a standard CMOS chip with bond-pads arranged in the matrix pattern. There are eight processing steps:

(1) Deposit a thick oxide layer on top of the chip. The thickness of this oxide layer must be at least 25 μm, since it will be used as a buffer layer during the dicing process afterwards (step 6).
(2) Make opening windows in the oxide layer to reach the bond-pads of the ASIC.
(3) Deposite aluminum into the opening windows to extend the conductive area to the surface of the oxide layer.
(4) Apply a layer of electrically conductive to connect all the bond-pads. The bond-pads are all temporarily shorted together. The grain size of

the conductive material in the glue must be smaller than the size of the opening window.

(5) Apply a piece of piezoelectric ceramic with golden electrodes on both sides[1] on top of the stack. The electrical connection between the bond-pads on the chip and the electrode on the back-side of the piezoelectric ceramic is obtained by means of the electrical conductive glue. For acoustic matching at the front-side of the piezoelectric ceramic, a piece of matching layer is applied.

(6) Separate the elements mechanically by means of a dicing process. The dicing kerfs are extended into the oxide layer for approximately 10 μm, which also electrically separates the elements.

(7) Glue a ground foil on top of the structure. All the transducer elements have their own connection to the silicon chip and one common ground.

(8) Add a backing layer at the back-side of the silicon chip.

Several positive features of the proposed method are summarized below:

- The vertical interconnection scheme results in a compact structure.
- The electrically conductive glue allows the room-temperature operation, which is clearly below the Curie temperatureduring the interconnection process.
- The electrically conductive glue is a frequently-used material for ultrasound transducer manufacturing (e.g. glue is usually applied to make the connection between piezoelectric transducer and flex circuits). The acoustic behavior of this material is well understood. The thickness of the glue layer can even be tuned to improve the acoustic matching.
- The dicing process is done after the adhesion of the transducer and the silicon chip. A chip with a thick oxide buffer layer provides a stable base for the dicing process to separate the transducer elements.

It is worth noting that the ASIC is in the acoustic path acts as a non-ideal backinglayer. It might degrade the image quality due to mechanical cross-

[1] The piezoelectric ceramic ordered by Oldelft B.V. has two golden electrodes attached to the top and bottom surfaces.

talk, and lower damping than an ideal backing layer would provide. Further investigation is required to address these issues.

## 7.4 Prototype Design

To demonstrate the effectiveness of the proposed interconnection method, experiments have been carried out. We firstly designed test chips with bond-pads in a matrix pattern at the DIMES Technology Center at TU Delft. These chips were post-processed to have top-oxide layers of 30 μm and an extended Aluminum contact area (shown as step 3 in Fig. 7.2). Next, the chips were processed by Oldelft UltrasoundB.V. for building transducers (step 4 to 8 of Fig. 7.2).

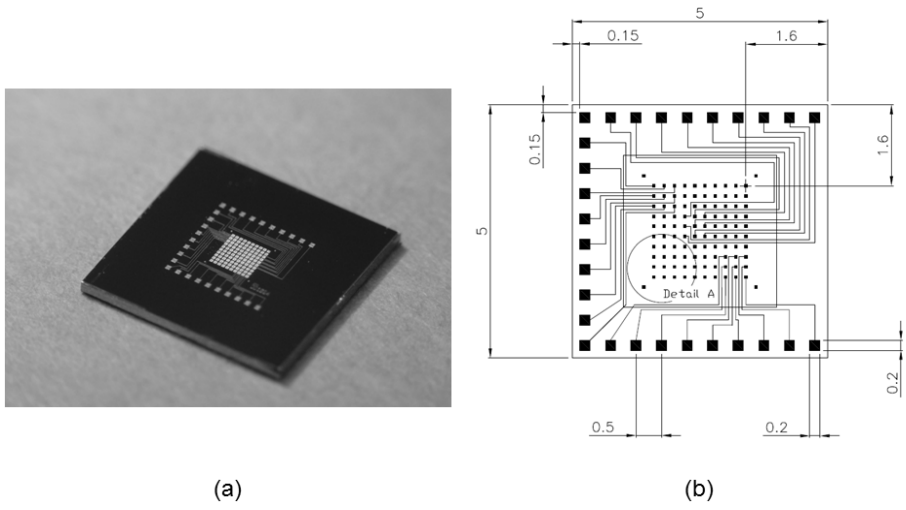


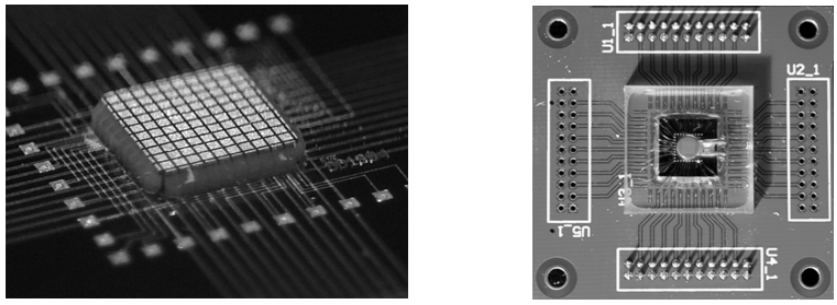

Fig. 7.3 The interconnection silicon test chip fabricated at DIMES: (a) chip photo (b) routing diagram.

Figure 7.3 shows a photo of a test chip (Fig. 7.3a) together with a drawing of the routing scheme (Fig. 7.3b). In the center of the test chip, there are 10 × 10 small bond-pads with a pitch of 200 μm. Three groups of 3 × 3 bond-pads are selected and routed via metal traces to big bond-pads on three sides of the chip. In this way, after building the transducer on the chip, we were able to check the connectivity of 27 transducer elements to the chip via these

large bond-pads. The resistance between a big bond-pad and an internal small bond-pad is about 10 Ω, which is negligible compare to the impedance of a transducer element.

Fig. 7.4a shows a piezo-stack that has been connected to the test chip and separated into small elements by a dicing process. The end-product of the interconnection test structure is shown in Fig. 7.4b, in which a ground foil was applied on top of the piezo-stack. A backing layer was attached to the back side of the chip as well. Next, the whole structure was glued to a PCB. Two small copper rods were connected to the ground foil and were soldered on a ground trace on the PCB. A protective layer was attached to the surface of the transducer array. Finally, the large bond-pads on the test chip were connected to the PCB board via wire bonding and epoxy is applied to protect the bond wires.

We have built two prototypes and a good yield has been achieved. For both prototypes, all 27 transducer elements can be accessed. Electrical impedance measurements have been carried out and the results for a group of 3 × 3 elements were discussed in section 2.3.2. All transducer elements work properly.




(a) (b)

Fig. 7.4 A matrix transducer assembled on the interconnection chip: (a) a piezo-stack is built on the chip and separated into small elements by a dicing process (b) the complete interconnection test structure (courtesy of Oldelft Ultrasound B.V.).

## 7.5 Conclusions

In this chapter, the technology of transducer-to-ASIC interconnection has been discussed and a novel method has been proposed. In this method, the vertical interconnection scheme results in a compact structure, which is desirable for 3D TEE application. Electrically conductive glue is used to form the interconnection, which allows room-temperature processing. Moreover, the acoustic property of the electrically conductive glue is well understood and the thickness of the glue layer can be tuned to optimize the acoustic performance. Transducer elements are separated after having been connected to the silicon chip. The chip with a relatively thick oxide layer works as a stable holder for the piezo-material during the dicing process. Test structures have been designed and fabricated and show a good yield. Impedance measurement shows that the transducer elements built on the test interconnection chip are working properly.

The research and development of the transducer-to-chip interconnection scheme is an important step in our project. The final goal of the project is to achieve fully integration of an ASIC and a matrix ultrasound transducer in a TEE probe for 3D echocardiography. In a true sense, the proposed interconnection scheme bridges up the transducer design and the electronics design. This enables our team to move one step further towards our final goal.

## 7.6 References

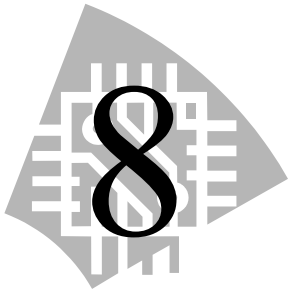
[7.1] CTS Corporate, "PZT5A & 5H Materials Technical Data", available at: http://www.ctscorp.com/components/pzt/downloads/PZT_5Aand5H.pdf

[7.2] B. Savord, R. Solomon, "Fully sampled matrix transducer for real time 3D ultrasonic imaging", *Proceedings IEEE Ultrasonics Symposium*, 2003, pp. 945-953.

[7.3] J.H. Lau, *Low Cost Flip Chip Technology for DCA, WLCSP, and PBGA Assemblies*, New York: McGraw-Hill, 2000.

[7.4] M.I. Fuller, E.V. Brush, M.D.C. Eames, T.N. Blalock, J.A. Hossack, W.F. Walker, "The sonic window: second generation prototype of low-cost, fully-integrated, pocket-sized medical ultrasound device", *Proceedings IEEE Ultrasonics Symposium*, 2005, pp. 273-276.

# *Conclusions*




The design of a miniature ultrasound probe for 3D Trans-Esophageal Echocardiography (TEE) is a multidisciplinary task, which involves transducer design, electronics design, ultrasound field analysis, mechanical design, etc. As part of the teamwork, this thesis has focused on two research topics. The first topic is the design of the receive ASIC, which will be used to provide appropriate signal processing to the signals received from a matrix ultrasound transducer with 45 × 45 elements in the tip of a TEE probe. The second topic is the transducer-to-ASIC interconnection methodology. In this final chapter, general conclusions of the thesis work are given and the main contributions to these two challenging research topics are summarized. Furthermore, suggestions for future research directions are given.

## 8.1 General Conclusions

### *Regarding the Front-End Receiver ASIC Design*

- To enable 3D TEE, a matrix transducer consisting of several thousands of elements is required. Smart signal processing, such as: channel-count reduction, by using an ASIC to interface the matrix transducer in the tip of a TEE probe is necessary.

- The separation of the transmit (Tx) and receive (Rx) transducer arrays highly simplifies the electronics design, since the high-voltage circuitry for the Tx array and the low-voltage circuitry for the Rx array are physically separated, without the need for protection circuitry. Moreover, the separation of the Tx/Rx arrays makes tissue harmonic imaging possible without the need for broadband transducer elements. Both Tx and Rx arrays can be optimized for their specific roles.
- The major challenges of the receive-ASIC design are the large element count of the Rx ultrasound transducer, the limited space in the TEE probe tip and the stringent power budget. Therefore, an effective front-end signal-processing scheme, and compact low-power circuitry are required.
- Instead of using a scheme for continuous time-gain compensation (TGC), the use of a four-step discrete-gain scheme [8.1] highly simplifies the TGC amplifier design.
- Micro-beamforming is an effective technique to reduce the channel count in the TEE probe tip. The micro-beamforming is done in such a way that the large matrix transducer is divided into sub-groups and delays are applied to the signals received by the transducer elements within a group to align them in time. Since elements in a sub-group are spaced close to each other, only fine delays are needed. These fine delays are possible to be realized by front-end electronics in the TEE probe tip.
- The use of the "pre-steering" technique [8.2] in the micro-beamforming scheme effectively changes the neutral beam direction of the transducer array by tilting all the groups to a certain angle. Although it introduces a small delay error with respect to an ideal element-wise beam steering, the advantage is that the electronics can be kept simple, because all the transducer sub-groups can share one delay configuration.
- The pipeline-operated S/H delay-line architecture [8.3][8.4][8.5] employed in the micro-beamformer offers several advantages that make it a suitable circuit block to be used for 3D TEE: low power, flexible, and accurate in terms of timing and gain. Residual charge-injection is the dominant error source that influences the precision of the S/H delay circuit.

- The charge-mode summation method combined with the pipeline-operated S/H delay structure intrinsically leads to circuits with low complexity and high power efficiency.
- Ultrasound receive front-end ICs with analog beamforming applied can achieve sub-mW power consumption per channel (section 5.4.5). This value is 1~2 orders-of-magnitude lower than front-end ICs using digital-beamforming.

### *Regarding the Transducer-to-ASIC Interconnection Methodology*

- The space in the TEE probe tip is limited (length: 2 cm; width: 1 cm; height: 1 cm). The most space-saving way of assembly is to have a vertical interconnection, i.e., stacking the ASIC and the Rx transducer.
- To avoid de-polarization of the piezo-material during the interconnection process, the assembly must be carried out at temperatures below the Curie point of the chosen piezo-material, i.e., 225ºC. The use of electrical-conductive glue allows room-temperature operation of the interconnection process. The thickness of the glue layer can be tuned to improve the acoustic matching of the transducer.
- The matrix transducer is made by dicing a piece of piezoelectric material in two orthogonal directions to separate the individual elements. The dicing process must be compatible with the interconnection process. A reasonable processing procedure is to apply the dicing process after the adhesion of the piezoelectric material and the ASIC. In this way, the ASIC acts as a stable holder. However, to prevent the ASIC from being damaged during the dicing process, a thick buffer layer on top of the ASIC is mandatory.

## 8.2 Main Contributions

### *Regarding the Receive-ASIC Design*

- The major challenges of the ASIC design have been identified (Chapter 1).

- The electrical properties of the Rx transducer have been characterized, such as the bandwidth, the noise floor, and the element-to-element sensitivity variations. Based on these characteristics, the boundary conditions and target specifications for the design of front-end electronics have been established (Chapter 2).
- System-level studies have been carried out to derive an effective scheme for processing of the receive signal in the ASIC (Chapter 3). The system-level study consists of two steps: Firstly, the architecture for the receive-signal processing has been designed. The ASIC is partitioned into three function blocks: low-noise amplifiers (LNAs), time-gain-compensation (TGC) amplifiers, and micro-beamforming circuitry. The micro-beamforming is implemented in such a way that the 45 × 45 transducer elements are divided into 225 sub-groups. Each sub-group consists of 3 × 3 elements and has its own micro-beamformer. Secondly, simplifications have been made to the function blocks, such as: the four-step discrete-gain scheme in the time-gain compensation and the pre-steering technique employed in the micro-beamforming scheme. Moreover, for further reduction of the complexity of the electronics, the required fine delay times have been approximated by a set of fixed delay steps. The optimal delay step size, which is 40 ns, has been derived by acoustic simulations. The delay ranges and patterns required to cover a cone-shape imaging space with a 90º opening angle have been calculated as well.
- Circuit solutions have been provided for the three function blocks (Chapter 4 & Chapter 5). Integrated-circuit prototypes of all the function blocks have been separately designed and measured. Firstly, the LNA has been implemented by a simple common-source amplifier with a resistive load. The circuit is extremely compact, has low noise and good power efficiency. Secondly, a low-power TGC amplifier has been designed using an open-loop topology with voltage-to-current (V/I) and current-to-voltage (I/V) converters [8.1]. Thirdly, the micro-beamformer has been realized using delay and summation in the analog domain. The analog delay lines have been designed using a pipeline-operated S/H delay architecture. Two micro-beamformers with different summation methods: current domain summation [8.4] and charge domain

summation [8.5] have been designed, implemented and tested. Charge-domain summation appeared to be favorable in view of simplicity and power efficiency.

- Two ultrasound receivers have been designed (Chapter 6). The first design is a 3-channel receiver implemented on a PCB [8.4]. While the second design is a 9-channel receiver ASIC. Both designs delivered proofs of concept and confirmed the effectiveness of the front-end signal-processing methodology in terms of channel-count reduction and power consumption.

### *Regarding the Transducer-to-ASIC Interconnection Methodology*

- The geometric and temperature constraints for the transducer-to-ASIC interconnection design have been identified (Chapter 2).
- An interconnection method has been proposed, which uses electrical conductive glue to form the conduction paths between the transducer elements and the ASIC (Chapter 7).
- The proposed interconnection method has been verified with experiments. Interconnection test chips with bond-pads in a matrix pattern have been built and post-processed. Afterwards, matrix transducers have been built on top of these test chips. Each test chip enables connectivity testing of 27 transducer elements to the chip. Measurements for two prototypes showed 100% yield. All the transducer elements showed proper impedances when being measured with an impedance analyzer (Chapter 7 & Chapter 2).

## 8.3 Future Research Directions

### *Regarding the Receiver-ASIC Design*

- Investigation of the influence of the ASIC on the image quality in terms of electrical performance
  - As discussed in Chapter 4, the LNA in the current design has limited linearity. Since the 2nd-harmonic-imaging technique is used, one

concern is that the fundamental signals will be distorted by the LNA and result in signal components in the 2nd-harmonic band. Further investigation is needed to judge to what extent this distortion will influence the image quality based on the 2nd-harmonic-imaging principle.

- The TGC amplifiers in the ASIC provide four discrete gain settings. Since the gain value and the timing are known, theoretically, in the external imaging system, all the output signals of the ASIC can be post-processed to restore their initial signal levels. One point of concern is the transient effect during the gain switching. Will the gain-switching transients introduce any undesirable visual effect on the ultrasound image? If so, what kind of post-signal processing can be applied to solve the problem?
- In the future, it is also important to study the need for a TGC amplifier in much more detail. Especially, we should concern the acoustic dynamic range in a TEE image.

- Further reduction of the power consumption of the ASIC

  The optimization in power consumption can be done hierarchically:
  - System-level optimization: As discussed in Chapter 3, the TGC amplifier is used to maintain the image uniformity and relaxes the dynamic-range requirements for the micro-beamforming circuitry. In Chapter 5, we have shown that the input-signal dynamic range of the micro-beamformer is limited by residual-charge-injection errors in the S/H delay line. Conceptually, if we would be able to reduce these errors using some circuit techniques, the input dynamic range of the micro-beamformer could be enhanced. In this way, the TGC amplifiers could be partially/fully eliminated. However, any extra circuit used to reduce the charge-injection error should consume considerably less power than the TGC amplifiers in the current design.
  - Circuit-level optimization: The LNA and the TGC amplifier can be optimized. For instance, the biasing circuitry can be shared among sub-groups. For the micro-beamformer circuit, the digital circuits dominate the power consumption. We could investigate an optimized implementation of the digital logic to reduce dynamic

power consumption. In addition, instead of operating all digital circuits at the full supply voltage, we could selectively operate part of the digital circuits at a lower supply voltage. Moreover, the layout of the digital circuits can be optimized to reduce the dynamic power consumptions associated with parasitic capacitances.

- Scaling up the current design to accommodate the full transducer array: When we scale up the circuit to accommodate the full transducer array with 45 × 45 Rx elements, the distribution of power lines, ground lines and the clock signals across the chip must be carefully designed. Moreover, it is essential that the influence of neighboring signal channels remain sufficiently low. This will require a good shielding scheme between the channels. Furthermore, the layout design must be optimized to match the pitch of the transducer elements. To enable the vertical interconnection with the Rx transducer elements, the chip must be equipped with bond pads in a matrix pattern and have a 1:1 mapping with the transducer elements. We need to explore the way of designing the ESD structures attached to the matrix-pattern bond pads on the ASIC, which should be compact yet robust enough to protect the circuit during the interconnection procedure.

### *Regarding the Transducer-to-ASIC Interconnection*

- Investigation of the influence of the ASIC on the image quality in terms of its acoustic properties**:** In the proposed transducer-to-ASIC interconnection scheme, the ASIC acts as a non-ideal backing layer. We need to investigate to what extent the ASIC will degrade the image quality due to mechanical crosstalk and lower damping than an ideal backing layer would provide. Finite-element-method (FEM) simulations are required to optimize the design and minimize the crosstalk.
- Building a matrix transducer on a fully integrated receiver ASIC: So far, to evaluate the effectiveness of the proposed interconnection scheme, test chips without any active circuitry but only metal routings have been used as the substrate material for transducer fabrication. In future work, we could build a matrix transducer directly on a fully integrated front-

end receiver ASIC. We should investigate how the mechanical stress generated during the chip post-process and the interconnection procedure might influence the performance of the receive circuitry.

## 8.4 References

[8.1] J. Yao, Z. Yu, M.A.P. Pertijs, G.C.M. Meijer, C.T. Lancée, J.G. Bosch, N. de Jong, "Design of a low power time-gain-compensation amplifier for a 2D piezoelectric ultrasound transducer", *Proceedings IEEE Ultrasonics Symposium*, 2010, pp. 841-844.

[8.2] S. Blaak, Z. Yu, G.C.M. Meijer, C. Prins, C.T. Lancée, J.G. Bosch, N. de Jong, "Design of a micro-beamformer for a 2D piezoelectric ultrasound transducer", *Proceedings IEEE Ultrasonics Symposium*, 2009, pp. 1338-1341.

[8.3] Z. Yu, M.A.P. Pertijs, G.C.M. Meijer, "A programmable analog delay line for micro-beamforming in a transesophageal ultrasound probe", *Proceedings IEEE International Conference on Solid-State and Integrated Circuit Technology*, 2010, pp. 299-301.

[8.4] Z. Yu, S. Blaak, Z. Chang, J. Yao, J.G. Bosch, C. Prins, C.T.Lancée, N. de Jong, M.A.P. Pertijs, G.C.M. Meijer, "Front-end receiver electronics for a matrix transducer for 3D transesophageal echocardiography", *IEEE Transaction on Ultrasonics, Ferroelectrics, and Frequency Control*, in press.

[8.5] Z. Yu, M. A. P. Pertijs and G. C. M. Meijer, "An ultrasound beamformer using pipeline-operated S/H delay stages and charge-mode summation," *Electronics Letters*, vol. 47, no. 18, pp. 1011-1012, Sept. 2011.

# Summary

This thesis describes the design of a front-end application-specific integrated circuit (ASIC), which will be put into the tip of a miniature ultrasound probe for 3D Trans-Esophageal Echocardiography (TEE). To enable 3D TEE, a matrix piezoelectric ultrasound transducer with more than 2000 elements will be used. Since a gastroscopic tube cannot accommodate the cables needed to connect all the transducer elements directly to an imaging system, local channel-count reduction is necessary. The main task of the ASIC is to provide appropriate signal conditioning in the tip of the probe to achieve channel-count reduction. The main goal of this thesis work is to design such an ASIC using simple, low-power circuits, while still maintaining good image quality. In addition to the electronics design, the interconnection between the matrix transducer and the ASIC is another important parallel research topic.

***Chapter 1 Introduction*** In this introductory chapter, the basic knowledge of TEE is given. This is followed by a short discussion on the challenges and choices in designing a 3D TEE probe. It is shown that in order to reduce the channel count and enhance signal quality from the output of an ultrasound matrix transducer, smart signal processing by using an ASIC in the tip of the probe is necessary. Meanwhile the circuits must be designed in such a way that they are compact and efficient enough to meet the stringent power and space requirements. Moreover, a new methodology is required to tackle the challenge of electrically connecting the transducer to the ASIC.

***Chapter 2 Ultrasound Transducers*** Ultrasound transducers are devices that are capable of converting energy between the mechanical domain and the electrical domain. They are indispensable elements in ultrasound imaging systems. In this chapter, a comprehensive description of piezoelectric ultrasound transducers is given. Several important characteristics associated with ultrasound signals have been discussed, such as the reflection at tissue boundaries, the propagation attenuation, signal dynamic range, and

harmonics generation. These form the foundations for ultrasound signal processing. The final part of this chapter is devoted to the analysis of the receive (Rx) transducer that is used in this thesis work. Its characteristics such as geometry, material, electrical model, bandwidth, and sensitivity variations have been studied. Based on the characteristics of this transducer, important implications have been derived on interconnection and the electronics design.

***Chapter 3 Front-End Receive-Signal Processing for 3D TEE*** In this chapter, a front-end signal-processing scheme for 3D TEE is presented. This signal-processing scheme will be realized by an ASIC. The ASIC consists of three function blocks: low-noise amplifiers (LNAs), time-gain-compensation (TGC) amplifiers and micro-beamformers. Since the ASIC is located in the tip of the TEE probe, its size and power consumption cannot be arbitrarily large. Therefore, the signal-processing scheme has been designed to be efficient enough to keep the ASIC compact and practically usable in a TEE probe. Provided that the image quality is not degraded, the signal-processing scheme should be as simpler as possible. To reduce the design complexity, we made simplifications to the TGC scheme and the analog-micro-beamforming scheme. Instead of using a continuous time-gain-compensation (TGC) scheme, the use of a four-step discrete-gain scheme greatly simplifies the TGC amplifier design. The micro-beamforming is done in such a way that the large matrix transducer is divided into sub-groups and delays are applied to signals received by transducer elements within a group to align them in time. The use of this "pre-steering" technique in the micro-beamforming scheme effectively reduces the circuit complexity.

***Chapter 4 LNA and TGC Amplifiers Design*** This chapter describes the designs of the LNA and the TGC amplifier. The LNA requires the lowest input-referred noise. It is likely the most power-hungry stage. To obtain a power-efficient implementation, we've chosen to use a simple open-loop single-ended topology. However, the simple open-loop topology of the LNA comes at the cost of large gain errors. Since the LNA and the TGC amplifier

are in cascading, the gain errors of the two circuit blocks add up. In order to ensure reasonable overall gain accuracy, we've chosen to allocate the majority of the gain-error budget to the LNA. Meanwhile, we've chosen to use a close-loop approach in the TGC amplifier in order to obtain a low enough gain-error contribution. Another limitation of the simple open-loop LNA is its poor linearity. One concern is the harmonic distortion due to the non-linear amplification. To relieve the problem caused by the poor linearity of the LNA, we've introduced the option of bypassing the LNA at high input-signal levels. Meanwhile, for the TGC amplifier design, we use local-feedback topology to achieve a high bandwidth while keeping the power consumption low. Several circuit techniques, such as: cascaded-flipped voltage followers (CASFVF) and Kelvin switches, have been employed to improve the accuracy. Prototypes of the LNA and the TGC amplifier have been manufactured and showed satisfying test results.

***Chapter 5 Micro-beamformer Design*** The beamforming principle is based on delaying the signals received by different transducer elements with respect to each other in such a way that signals received from the focal point are aligned in time and can be coherently summed. In this chapter, we focus on the circuit implementations of the micro-beamforming scheme (proposed in Chapter 3). In principle, a micro-beamformer can either be implemented in the analog domain or in the digital domain. For our specific application, analog beamforming is chosen for its power efficiency. To realize analog delays, a so-called "pipelined sampled delay" principle has been chosen. Based on this principle, a pipeline-operated S/H delay structure is introduced. Design aspects that limit the precision of the S/H delay-line are explored, such as: residual charge injection, residual clock-feed-through error and *kT/C* noise, have been discussed and analyzed. It is shown that the residual charge-injection is the dominant error source. Furthermore, signal-summation methods in the current domain and in the charge domain are investigated. For performance evaluation, two prototype chips with the same delay line topology but different signal summation methods (current domain and charge domain) have been designed and fabricated. Both prototypes meet the design requirements. The prototype chip with the charge-mode

summation method shows an even better power efficiency compared to the prototype chip with current-mode summation.

***Chapter 6 Ultrasound Receiver Realizations*** In this chapter, two ultrasound receivers have been presented. The first design is a 3-channel receiver implemented on a PCB. Measurement results of this receiver confirm the effective functionality of the signal-processing chain. Based on the promising results obtained with the PCB demonstrator, a 9-channel receiver ASIC has been designed and fabricated. This 9-channel receiver chip has been used to readout 3 × 3 Rx transducer elements. Measurements show that the ASIC is capable of processing real ultrasound echo signals effectively.

***Chapter 7 Transducer-to-ASIC Interconnection Method*** In addition to the circuit design, how to electrically connect the ASIC to the matrix ultrasound transducer is another great challenge. In this chapter, a novel interconnection method has been proposed. In this method, the vertical-interconnection scheme results in a compact structure. Electrical-conductive glue is used to form the interconnection, which allows room-temperature processing. Test structures have been designed and fabricated and show a good yield. Impedance measurement shows that the transducer elements built on the test interconnection chip work properly.

# Samenvatting

Dit proefschrift beschrijf het ontwerp van een toepassingsspecifieke geïntegreerde schakeling (ASIC) die geplaatst zal worden in de tip van een miniatuur ultrageluid probe voor 3D Trans-Esophagale Echocardiografie (TEE). Om 3D TEE mogelijk te maken zal een piëzoelektrische ultrasone matrixtransducent met meer dan 2000 elementen worden gebruikt. Een gastroscopische buis kan niet alle draden bevatten die nodig zijn voor de verbinding van deze transducent met het echoapparaat. Daarom moet er electronica in de tip van de transducent worden geïntegreerd, middels een zogenaamde ASIC (Application Specific Integrated Circuit). Het belangrijkste doel van het onderzoek beschreven in dit proefschrift is om zo'n ASIC te ontwerpen waarbij gebruik wordt gemaakt van eenvoudige laagvermogen circuits die toch een goede beeldkwaliteit opleveren. In aanvulling hierop vormt ook de verbinding tussen de ASIC en de matrixtransducent een belangrijk onderdeel van het onderzoek.

***Hoofdstuk 1 Introductie*** Dit inleidende hoofdstuk behandelt basiskennis over TEE. Daarna volgt een korte discussie over de uitdagingen en keuzes bij het ontwerp van een 3D TEE probe. Er wordt aangetoond dat, teneinde het aantal kanalen te reduceren en de kwaliteit van het uitgangssignaal van de matrixtransducent te verbeteren, het nodig is om in de tip van de probe gebruik te maken van een ASIC voor slimme signaalbewerking. Tegelijkertijd dienen de circuits zodanig te worden ontworpen dat ze voldoende compact en efficiënt zijn om te kunnen voldoen aan de strenge eisen betreffende vermogens- en ruimteverbruik. Bovendien is nieuwe technologie nodig om het uitdagende probleem van de transducent-ASIC verbinding op te kunnen lossen.

***Hoofdstuk 2 Ultrasone Transducenten*** Ultrasone transducenten zijn elementen die energie van het mechanische naar het elektrische domein en v.v. kunnen converteren. Ze zijn onmisbaar voor ultrasone beeldverwerkende systemen. In dit hoofdstuk worden piëzoelektrische transducenten uitgebreid beschreven. Verschillende belangrijke kenmerkende eigenschappen van ultrasone signalen worden besproken, zoals

reflectie op weefselgrenzen, voortplantingsverzwakking, dynamisch bereik, en generatie van harmonische signalen. Deze eigenschappen vormen de basis voor ultrasone signaalbewerking. Het laatste deel van dit hoofdstuk is gewijd aan de analyse van de ontvangst(Rx)transducent die voor dit promotieproject is gebruikt. Kenmerkende eigenschappen zoals geometrie, materiaal, elektrisch model, bandbreedte, en gevoeligheidsvariaties zijn bestudeerd. Gebaseerd op deze eigenschappen worden belangrijke gevolgtrekkingen gemaakt voor verbindingen en elektronisch ontwerp.

***Hoofdstuk 3 Bewerking van het ontvangstsignaal in het ingangsdeel van een 3D TEE probe*** In dit hoofdstuk wordt een concept gepresenteerd voor de signaalbewerking in het ingangsgedeelte van een 3D TEE probe. Dit signaalbewerkingsschema wordt gerealiseerd in een ASIC die bestaat uit drie functieblokken: ruisarme versterkers (LNAs), versterkers voor tijd-versterking compensatie (TGC), en microbundelvormers. Daar de ASIC zich bevindt in de tip van de TEE probe, kunnen omvang en vermogensverbruik niet willekeurig groot zijn. Bij het ontwerp van het signaalbewerkingsschema is hiermee rekening gehouden. Vooropgesteld dat de beeldkwaliteit er niet onder mag leiden, is dit schema zo eenvoudig mogelijk gehouden. Om de ontwerpcomplexiteit te verminderen, hebben we de manier van tijd-versterking compensatie en bundelvorming vereenvoudigd. In plaats van gebruik te maken van continue tijd-versterking compensatie (TGC), blijkt het gebruik van TGC met slechts vier discrete versterkingsstappen het ontwerp zeer te vereenvoudigen.

De microbundelvorming wordt op zodanige wijze uitgevoerd dat de grote matrixtransducent wordt verdeeld in subgroepen waarbinnen middels onderlinge tijdsvertragingen de signalen zijn “uitgelijnd”, zodat de vertraagde signalen afkomstig zijn van een bepaald focuspunt op hetzelfde moment van reflectie. Het gebruik van deze “pre-steering” techniek in de bundelvormers leidt tot een aanzienlijke vermindering van de complexiteit van de schakelingen.

***Hoofdstuk 4 Het ontwerp van de LNA en de TGC versterker*** Dit hoofdstuk beschrijft het ontwerp van de LNA en de TGC versterker. Omdat de LNA het meest ruisarm moet zijn, verbruikt hij waarschijnlijk het meeste

vermogen. Om een vermogenszuinige uitvoering te verkrijgen is gekozen voor het gebruik van een eenvoudige open-lus versterkertopologie met enkelzijdige uitgang. De open-lus topologie leidt echter tot grote fouten in de versterkingsfactor. Daar de LNA en de TGC versterker zijn gecascadeerd, zullen fouten in de versterkingsfactoren bij elkaar optellen. Voor wat betreft het foutenbudget hebben we ervoor gekozen om de grootste deel ervan toe te kennen aan de LNA. Tegelijkertijd hebben we er voor gekozen om voor de TGC versterker een gesloten-lus benadering te kiezen, waardoor de foutbijdrage in de versterkingsfactor beperkt blijft. Een andere beperking van de eenvoudige LNA betreft zijn slechte lineariteit. Een punt van zorg betreft de harmonische vervorming die hiervan het gevolg is. Om het probleem veroorzaakt door de slechte lineariteit van de LNA te verminderen, hebben we een optionele omleiding voor de LNA aangebracht, die gebruikt wordt bij hoge signaalniveaus. Verder gebruiken we voor de TGC versterker de topologie van lokale terugkoppeling om daarmee een hoge bandbreedte te verkrijgen en daarbij het vermogensverbruik laag te houden. Voor het verkrijgen van een hoge nauwkeurigheid hebben we verschillende technieken gebruikt, zoals: cascoded-flipped spanningsvolgers (CASFVF) en Kelvin schakelaars. Prototypen van de LNA en de TGC versterker zijn ontworpen en vervaardigd en laten bevredigende testresultaten zien.

***Hoofdstuk 5 Het ontwerp van Microbundelvormers*** Het principe van bundelvorming is gebaseerd op het onderling vertragen van de signalen die door de verschillende transducentelementen worden ontvangen. Dit gebeurt op zodanige wijze dat de ontvangen signalen afkomstig van een bepaald focuspunt worden “uitgelijnd” in tijd zodat ze coherent kunnen worden opgeteld. In dit hoofdstuk, richten we ons op circuituitvoeringen voor de microbundelvorming (zoals eerder voorgesteld in Hoofdstuk 3). In principe kan een microbundelvormer worden uitgevoerd in zowel het analoge als het digitale domein. Voor onze toepassing is analoge bundelvorming gekozen vanwege het lage vermogensverbruik. Voor het realiseren van analoge vertragingen is gekozen voor het principe van “pijplijn-bemonsterde vertraging”. Uitgaande van dit principe is een pijplijn S/H vertragingsstructuur geïntroduceerd. Ontwerpaspecten betreffende de nauwkeurigheid van de S/H vertragingslijnen zijn verkend. Met name

resterend ladingsinjectie, resterende overspraak van kloksignalen en *kT/C* ruis worden besproken en geanalyseerd. De dominante foutbron blijkt te worden gevormd door resterende ladingsinjectie. Verder zijn methoden onderzocht voor de sommatie van signalen in zowel het stroom- als het ladingsdomein. Ten behoeve van een experimentele evaluatie van de eigenschappen zijn twee prototypen van chips gemaakt voor beide wijze van signaaloptelling (in het stroom- en in het ladingsdomein). Beide prototype voldoen aan de gestelde eisen. De prototypechip die werkt in het ladingsdomein werkt echter beter dan die welke werkt in het stroomdomein.

***Chapter 6 Realisaties van de ultrasone ontvanger*** In dit hoofdstuk worden twee ultrasone ontvangers voorgesteld. De eerste is een 3-kanaals ontvanger uitgevoerd op Printed-Circuit Board (PCB). Meetresultaten van deze ontvanger bevestigen de doelmatige functionaliteit van de signaalbewerkingsketen. Vanwege de veelbelovende resultaten die met dit ontwerp zijn behaald is daarna een 9-kanaalsversie van de ontvanger als ASIC ontworpen en vervaardigd. Deze 9-kanaals ontvangerchip is gebruikt voor het uitlezen van een matrixtransducent met $3 \times 3$ elements. Metingen laten zien dat de ASIC in staat is om ontvangen ultrasone echosignalen op doelmatige wijze te bewerken.

***Hoofdstuk 7 Transducent-ASIC Verbindingsmethode*** Naast het schakelingontwerp vormt ook het ontwerp van de elektrische verbinding tussen ASIC en matrixtransducent een grote uitdaging. In dit hoofdstuk wordt een nieuwe verbindingsmethode voorgesteld. Bij deze methode resulteert een verticale verbinding in een compacte structuur. Elektrisch-geleidende lijm vormt de verbinding, hetgeen bewerking bij kamertemperatuur mogelijk maakt. Proefstructuren zijn ontworpen en vervaardigd en laten een goede opbrengst zien. Impedantiemetingen laten zien dat de transducentelementen die zijn verbonden zijn met de verbindingschip goed werken.

# Appendix A: Simulated Spatial Sensitivity of a Receive-Matrix Transducer with Pre-steering and Discrete Delays

All the simulations were carried out using the program Field II [A.1][A.2] . We considered a receive-matrix transducer consisting of 45 × 45 elements, arranged in 15 × 15 groups of 3 × 3 elements, with an element pitch of 200 μm (Fig. 3.2 on page 45). The responses of the array were calculated for a measurement grid of 201 × 201 point-source locations at 4 different depths (30 mm, 60 mm, 100 mm and 150 mm). The point source emits a 6 MHz pulse, which is generated as the second harmonic from an original 3 MHz transmit pulse with a Gaussian envelope and a 50% bandwidth (Fig. A.1).

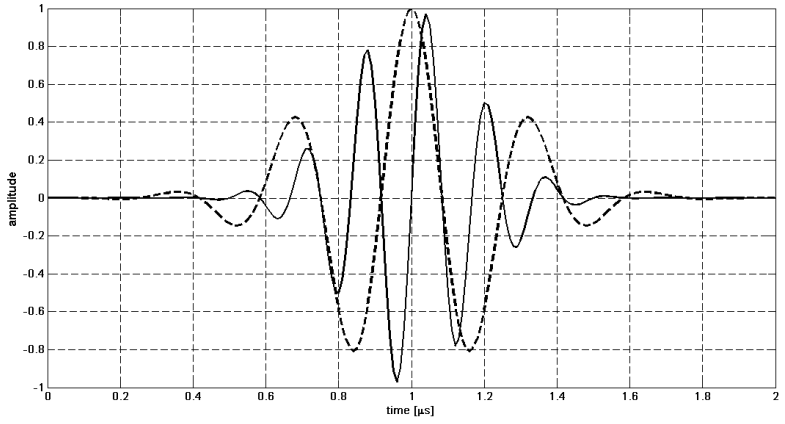



Fig. A.1 The point source used in the acoustic simulation (Dotted line: the transmitted pulse, 3MHz, Gaussian envelope and 50% bandwidth. Solid line: generated second harmonic, 6MHz and 35% bandwidth. ) (Courtesy of Dr. C.T. Lancée)

A diagram of the matrix transducer configuration and the signal-processing scheme are shown in Fig. A.2.

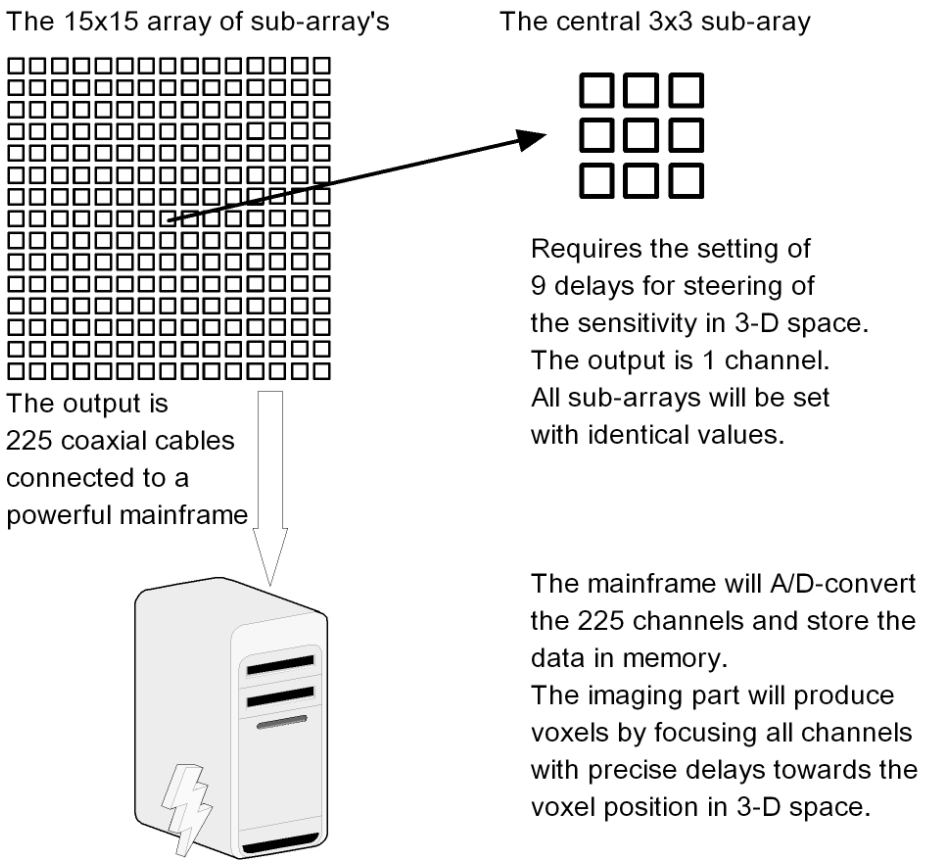



Fig. A.2 Diagram of the matrix transducer configuration (Courtesy of Dr. C.T. Lancée).

As shown in Fig. A.2, each sub-array requires the setting of 9 fine delays within the group. Two cases have been considered:

Case I: All nine elements in each sub-array have their exact "ideal" fine delays.

Case II: All nine elements within a sub-group are assigned with "discrete" fine delays, which consist of rounded values in the form of multiples of 40 ns.

For both cases I and II, pre-steering is applied, i.e., all 15 × 15 sub-arrays have the same fine-delay pattern. Afterwards, coarse delays are applied to the output signals from all 15 × 15 sub-arrays to achieve the beam-focusing.

Since these coarse delays are generated in a powerful mainframe, they can be made rather precise.

### *Description of the simulation steps*[1]:

(1) Define the array configuration, size, kerf and pitch of all elements in the plane z = 0.
(2) Define the values for the steering angles θ and φ. Focus will be infinite[2].
(3) Calculate the fine delays of all 9 elements of the centre sub-group to achieve this steering.
(4) Define a measurement plane at z = 30 mm, 60 mm, 100 mm or 150 mm.
(5) The measurement grid is 201 × 201 points[3].
(6) Using Field II to calculate the impulse response of each sub-group element for all grid points.
(7) Correct the impulse responses for the steering delay values.
(8) The impulse response of the sub-group is obtained by summation.
(9) The waveform response is obtained by a convolution with the impulse response.
(10) Steps (6) to (9) are repeated for all 224 other sub-groups using the same fine-delay pattern.
(11) Define a focus point in the grid.
(12) Calculate the focus delays to focus the 225 sub-group centres to this focus point.
(13) Correct the sub-group time signals for the focus delays.
(14) Summation of (13) yields a time signal for each grid point.

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[1] The simulation steps are valid for both case I and case II.

[2] Infinite focusing for each sub-group is chosen in order to achieve a large depth of field.

[3] To show the sensitivity distribution in space, two measurement grids have been used. Both grids consist 201 × 201 points.
Measurement grid A: This grid covers the whole scanning area at a given distance. This shows the existence of spurious lobes far away from the focal area.
Measurement grid B: This grid is a 20 mm × 20 mm square and is centred on the focus point. This shows the focal area in greater detail.

(15) Assigning the maximum amplitude of (14) to each grid point yields a plot of the sensitivity distribution over the grid.

In the next 6 figures, typical simulation results show the performance of the application of pre-steering and discrete delays to the matrix array.

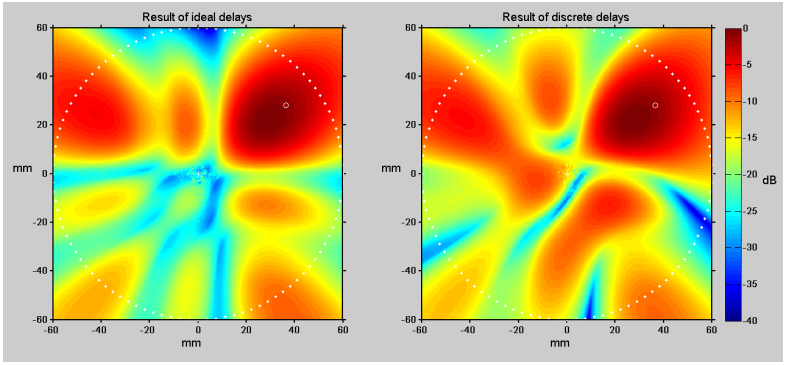


Fig. A.3 Example: The spatial sensitivity distribution of the central 3 × 3 sub-array at 60 mm, with steering direction 52.5º elevation and 37.5º azimuth (left: Case I; right: Case II). Measurement grid A (see footnote 3 on page 161) is used and the scanning volume is displayed as a white-dotted circle. It can be seen that discrete delays in case II result in slightly different sensitivity distribution compared to the ideal delays in case I. (Courtesy of Dr. C.T. Lancée)

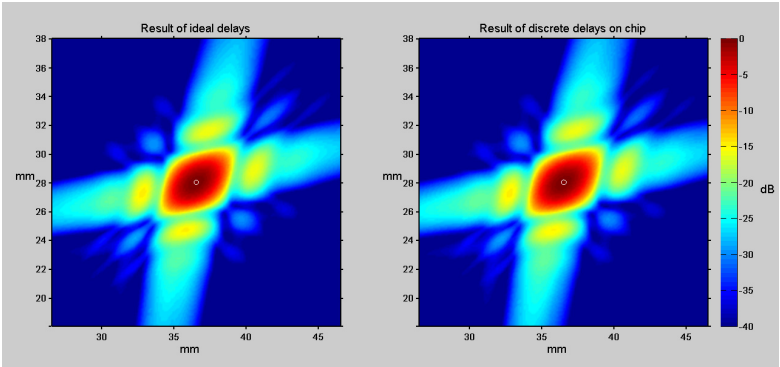


Fig. A.4 Example : A close view of the spatial sensitivity distribution of the full 45 × 45 matrix array at 60 mm, with steering direction 52.5º elevation and 37.5º azimuth (left: case I; right: case II). The 225 channels are focused on the intersection of the steering direction from the center of the array with the plane at 60 mm. Measurement grid B (see footnote 3 on page 161) is used. It can be seen that in case II with discrete delays applied, the resulting sensitivity distribution at the focus point is similar to case I, in which ideal delays are applied. (Courtesy of Dr. C.T. Lancée)

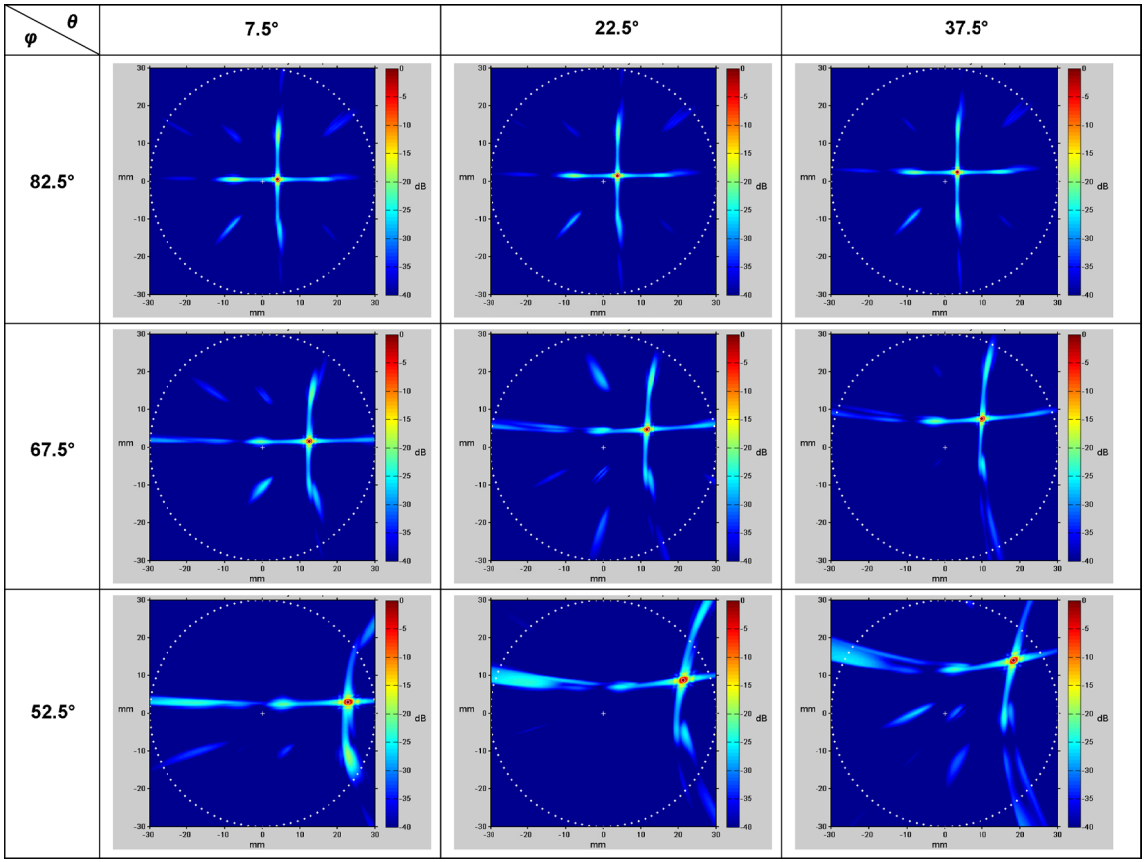


Fig. A.5 The spatial sensitivity distribution of the 45 × 45 matrix transducer at 30 mm and various steering angles (azimuth angle: θ and elevation angle: φ). Measurment grid A is used (see footnote 3 on page 161) and the scanning volume is displayed as a white-dotted circle. (Courtesy of Dr. C.T. Lancée)

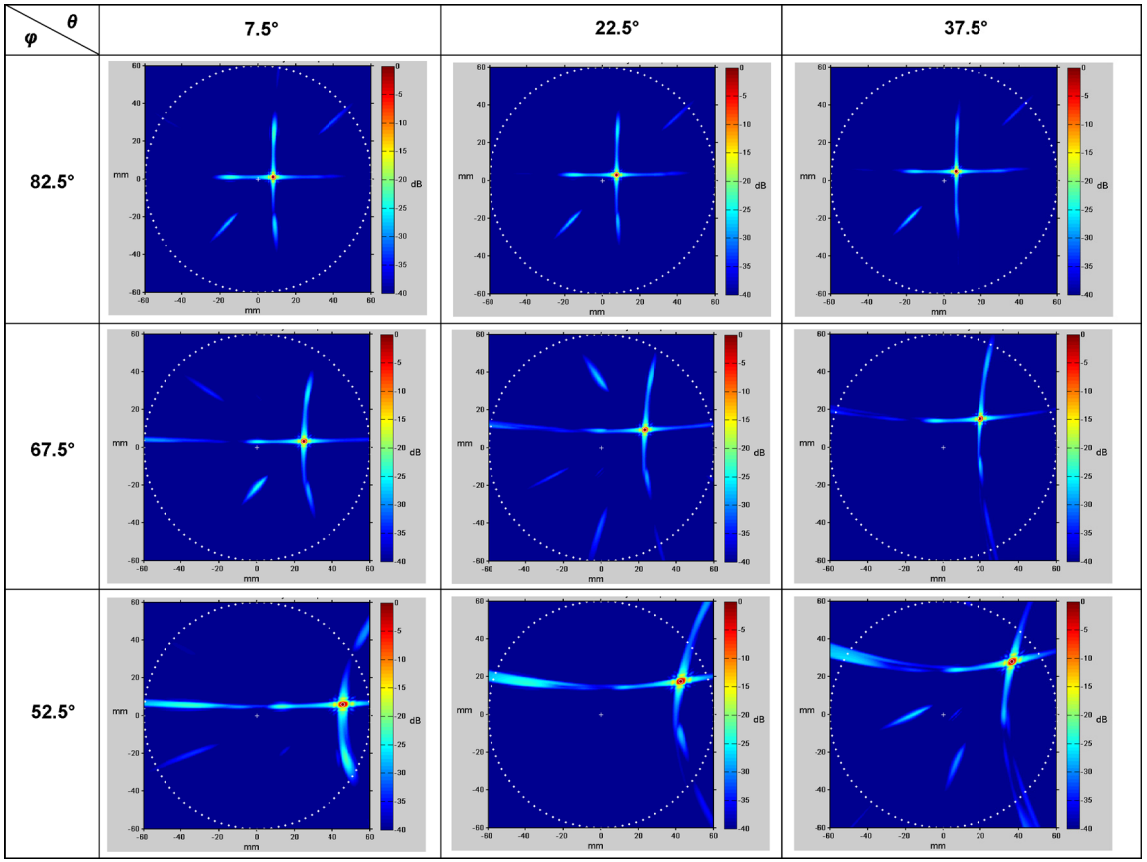


Fig. A.6 The spatial sensitivity distribution of the 45 × 45 matrix transducer at 60 mm and various steering angles (azimuth angle: θ and elevation angle: φ). Measurment grid A is used (see footnote 3 on page 161) and the scanning volume is displayed as a white-dotted circle. (Courtesy of Dr. C.T. Lancée)

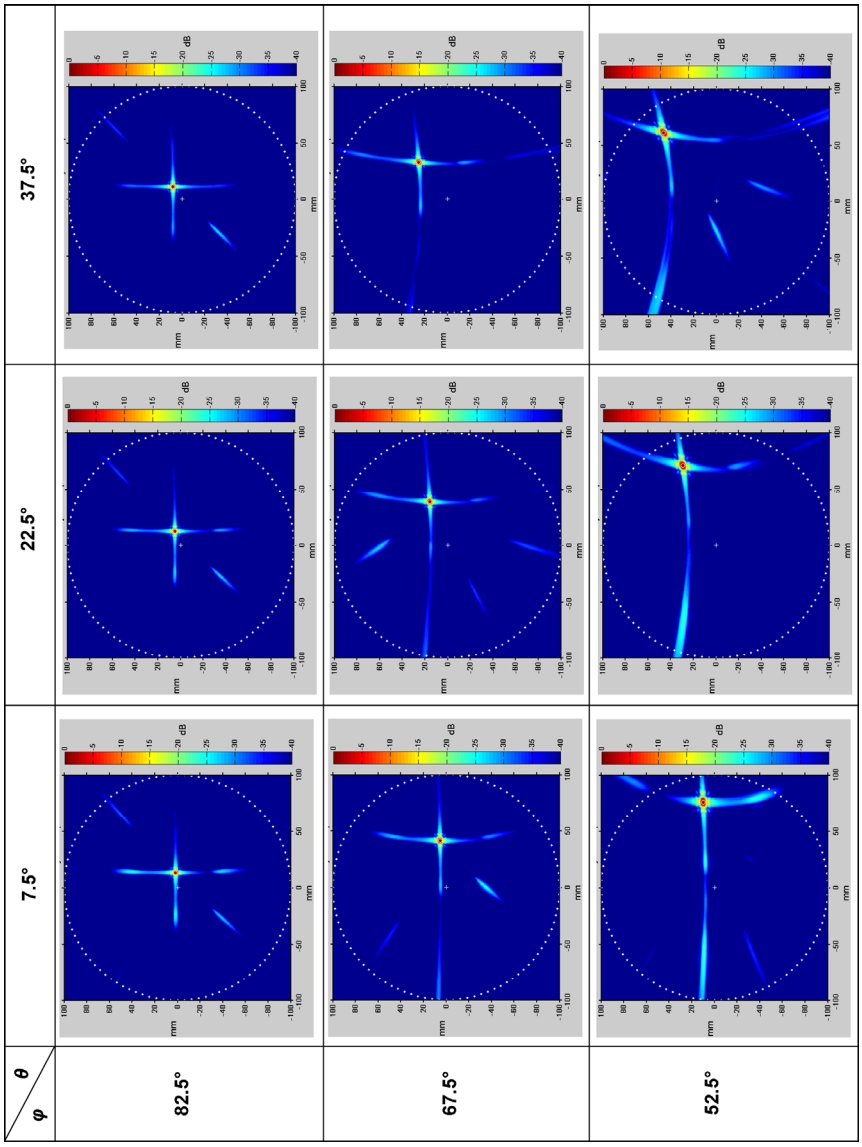


Fig. A.7 The spatial sensitivity distribution of the 45 × 45 matrix transducer at 100 mm and various steering angles (azimuth angle: θ and elevation angle: φ). Measurment grid A is used (see footnote 3 on page 161) and the scanning volume is displayed as a white-dotted circle. (Courtesy of Dr. C.T. Lancée)

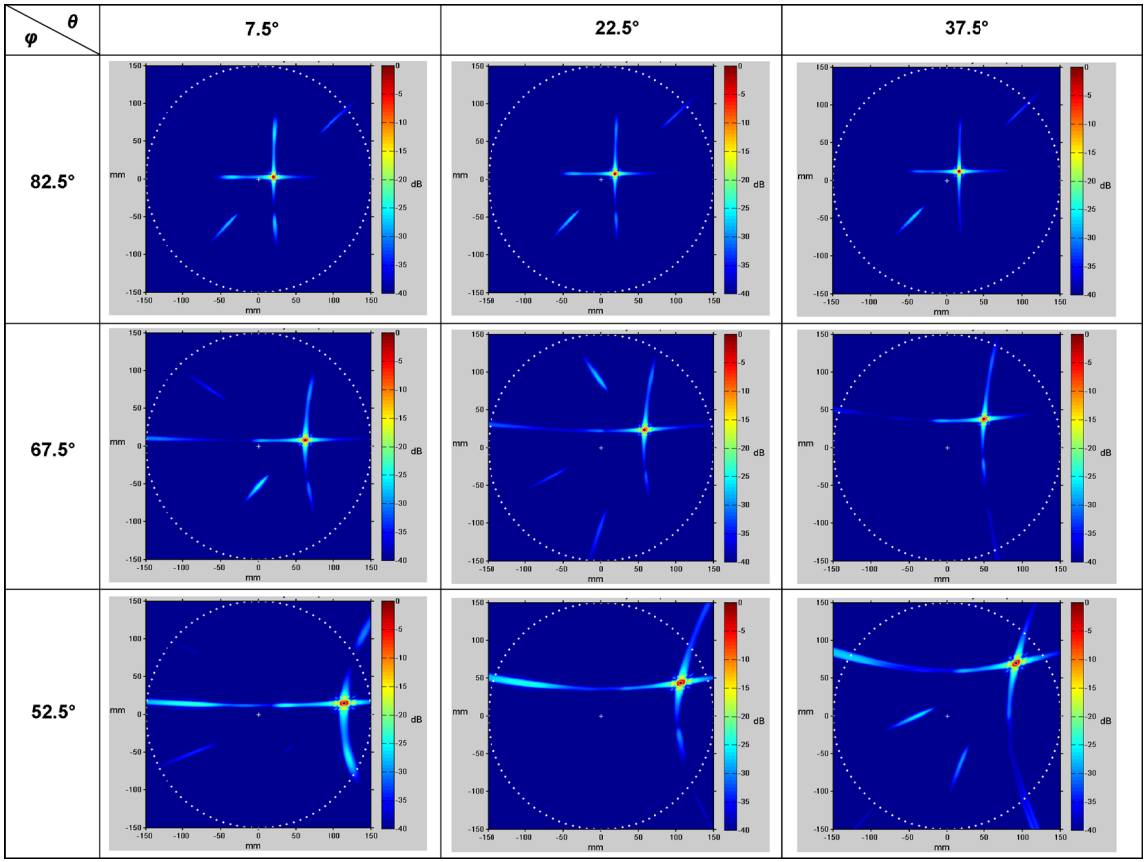


Fig. A.8 The spatial sensitivity distribution of the 45 × 45 matrix transducer with focus at 150 mm and various steering angles (azimuth angle: θ and elevation angle: φ). Measurment grid A is used (see footnote 3 on page 161) and the scanning volume is displayed as a white-dotted circle. (Courtesy of Dr. C.T. Lancée)

TABLE A.1 MAXIMUM SENSITIVITY AT DIFFERENT IMAGING DEPTHS FOR VARIOUS ELEVATION ANGLES φ AND AZIMUTH ANGLES θ. (COURTESY OF DR. C.T. LANCÉE)

| **Steering angle** | | **Maximum Sensitivity (dB)** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **φ (°)** | **θ (°)** | **30 mm** | | **60 mm** | | **100 mm** | | **150 mm** | |
| | | **case I** | **case II** | **case I** | **case II** | **case I** | **case II** | **case I** | **case II** |
| 82.5 | 7.5 | -0.26 | -3.07 | -0.30 | -2.07 | -0.07 | -1.62 | -0.26 | -1.75 |
| 82.5 | 22.5 | -0.25 | -2.72 | -0.30 | -1.68 | -0.05 | -1.20 | -0.27 | -1.33 |
| 82.5 | 37.5 | -0.24 | -2.55 | -0.29 | -1.47 | -0.05 | -0.98 | -0.26 | -1.11 |
| 67.5 | 7.5 | -1.88 | -3.90 | -1.92 | -3.14 | -1.71 | -2.75 | -1.93 | -2.91 |
| 67.5 | 22.5 | -1.88 | -3.97 | -1.92 | -3.13 | -1.73 | -2.74 | -1.94 | -2.89 |
| 67.5 | 37.5 | -1.87 | -3.24 | -1.91 | -2.43 | -1.72 | -2.05 | -1.93 | -2.20 |
| 52.5 | 7.5 | -5.11 | -6.43 | -5.25 | -6.15 | -5.06 | -5.87 | -5.28 | -6.06 |
| 52.5 | 22.5 | -5.04 | -5.92 | -5.19 | -5.54 | -4.99 | -5.23 | -5.22 | -5.42 |
| 52.5 | 37.5 | -5.00 | -6.42 | -5.13 | -6.07 | -4.94 | -5.77 | -5.16 | -5.96 |

* Reference of the sensitivity at each imaging depth is the maximum sensitivity at elevation angle φ = 90° with ideal delays applied. All delays in the sub-groups are 0 in this case. Focus point is on the intersection of the z-axis and the corresponding measurement plane.

General results of applying discrete delays compared to the ideal delay case:

(1) The sensitivity at the focus point becomes slightly lower.
(2) More spurious components due to increased grating effects. As indicated in Section 3.2.2.2, grating lobe level should be kept at least -20 dB lower than the main lobe level.
(3) Lower side-lobe levels are expected, because of the reduced interference efficiency.

# References

[A.1] J.A. Jensen, "Field: A Program for Simulating Ultrasound Systems", *Medical & Biological Engineering & Computing,* vol. 34, supplement 1, part 1, pp. 351-353, 1996.

[A.2] J.A. Jensen, N. B. Svendsen, "Calculation of pressure fields from arbitrarily shaped, apodized, and excited ultrasound transducers", *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control,* vol. 39, issue. 2, pp.262-267, 1992.

# List of Publications

## *Peer-reviewed articles*

**Z. Yu**, M. A. P. Pertijs and G. C. M. Meijer, "An ultrasound beamformer using pipeline-operated S/H delay stages and charge-mode summation," *Electronics Letters*, vol. 47, no. 18, pp. 1011-1012, Sept. 2011.

**Z. Yu**, S. Blaak, Z. Chang, J. Yao, J.G. Bosch, C. Prins, C.T.Lancée, N. de Jong, M.A.P. Pertijs, G.C.M. Meijer, "Front-end receiver electronics for a matrix transducer for 3D transesophageal cchocardiography", *IEEE Transaction on Ultrasonics, Ferroelectrics, and Frequency Control*, in press.

## *Conference proceedings*

J. Yao, **Z. Yu**, M.A.P. Pertijs, G.C.M. Meijer, C.T. Lancée, J.G. Bosch, N. de Jong, "Design of a low power time-gain-compensation amplifier for a 2D piezoelectric ultrasound transducer", *Proceedings IEEE Ultrasonics Symposium*, San Diego, The USA, Oct. 2010.

**Z. Yu**, M.A.P. Pertijs, G.C.M. Meijer, "A programmable analog delay line for micro-beamforming in a transesophageal ultrasound probe", *Proceedings IEEE International Conference on Solid-State and Integrated Circuit Technology*, Shanghai, China, pp. 299-301, Nov. 2010.

S. Blaak, **Z. Yu**, G.C.M. Meijer, C. Prins, C.T. Lancée, J.G. Bosch, N. de Jong, "Design of a micro-beamformer for a 2D piezoelectric ultrasound transducer", *Proceedings IEEE Ultrasonics Symposium*, Rome, Italy, pp.1338-1341, Sept. 2009.

**Z. Yu**, G.C.M. Meijer, C. Prins, N. de Jong, J.G. Bosch, "Design constraints of the interface electronics for an ultrasonic matrix transducer for 3D

transesophageal echocardiography", *Proceedings Sense of Contact*, Zeist, The Netherlands, Apr. 2008.

**Z. Yu**, G.C.M. Meijer, "A programmable time-gain-compensation (TGC) amplifier for medical ultrasonic echo signal processing", *Proceedings IEEE International Conference on Solid-State and Integrated Circuit Technology*, Beijing, China, pp. 1725-1728, Oct. 2008.

**Z. Yu**, G.C.M. Meijer, "The interface electronics for an ultrasonic matrix transducer for 3D transesophageal echocardiography*", Proceedings Electronics'2008*, Sozopol, Bulgaria, vol.3, pp. 19-22, Sept. 2008.

## *Workshop Contributions*

**Z. Yu**, "Imaging the heart with ultrasound", Invited talk, Sense of Contact workshop 13, Zeist, the Netherlands, Apr. 2011.

**Z. Yu**, et al. "Imaging the heart with ultrasound", Poster presentation, DIMES DAY 2011, TU DELFT, June. 2011. (***best poster award***)

**Z. Yu**, S. Blaak, G.C.M. Meijer, M.A.P. Pertijs, C.T. Lancée, H. Bosch, C. Prins, N. de Jong, "Design of a beamformer for an ultrasonic matrix transducer for 3D transesophageal echocardiography," Sense of Contact workshop 12, Apr. 2010. (***best poster award***)

# Acknowledgements

This thesis work would not be done without the help and support from many people. I would like to take this opportunity to express my gratitude to all of them. First of all, I would like to thank members from the pieken-in-de-delta (PID) project group: Thanks Prof. Gerard Meijer for accepting me as his PhD student to work on this interesting project. Thanks for his advices, support, encouragement and care during my PhD life. Thanks Dr. Michiel Pertijs for all insightful comments and suggestions on my designs and thesis writing. Thanks Prof. Nico de Jong, Dr. Hans Bosch, Dr. Charles Lancée and Ir. Sandra Blaak from ErasmusMC for guiding me to the ultrasound world and for all important discussions and feedbacks on my work and thesis writing. Thanks Ruud't Hoen, Christian Prins and Jacco Ponte from Oldelft Ultrasound B.V. for all support on transducer manufacturing and other project related issues. Thanks Ir. Libetario Demi, Dr. Martin Verweij and Dr. Koen van Dongen from the Physics Department, TUD, for discussions on ultrasound-field analysis. I really appreciate the cooperation in our PID project group and it has been a great experience.

I am grateful to people who have helped me during my journey towards getting my thesis finished. Thanks Prof. Lis Nanver and her group for their support on the transducer-to-ASIC interconnection design. Thanks Zu-yao Chang from Electronic Instrumentation Lab, TUD, for supporting on chip measurement and design-software maintainance. Thanks our MSc student Jiajian Yao for his effort added to this project. Thanks Paul van Neer and Robert Beurskens from ErasmusMC for their help on design issues related to ultrasound transducer and system. Thanks Greta Milczanowska, Kurt van Genechten and Robin Brouns from Europractice, and Ivan Koudar from ON Semiconductor, for answering many questions related to the IC process. Thanks Wil Straver from ELCA lab, TUD, for suggestions on bonding issues of the interconnection test chip. Thanks Prof. Ronald Dekker for suggestions on interconnection design at the early stage of the project. Thanks Prof. Alle-jan van der Veen for discussions on array-signal processing.

As a member of the Electronic Instrumentation Lab, I had a nice time stay in this “big family”. I appreciate the support from staff members: Kofi, Paddy, Joyce, Willem, Piet, Jeroen, Stoyan, Ger, Jeff and Antoon. I’d like to thank my old and new colleagues: Jia Qi, Caspar, Mahdi, Sha Xia, Chung-Kai, Yue Chen, Lei Shi, Huaiwen, Saleh, Qinwen, Ning, Mohammad, Ali Heidary, Zhichao, Ruimin, Lukasz, Gayathri, Sharma, Agung, Youngcheol, Eduardo, Maureen, Vijay, Deva, Martijn, Frerik, Rong, Paulo and André, for many chats over technical and non-technical topics. I am also grateful to Dr. Li and Dr. Wang for their support and care in the past years.

My office room is next door to the Lab of Electromagnetic Research. I would like to thank old and new members from the EM lab: Prof. Adrianus de Hoop, Martin, Xiaoyan, Jianing, Shreyas, Rob, Koos and Neil, for many pleasant corridor chats.

I would like to thank many other friends: Chen Wei, Chen Bin, Liu Rui, Wei Jia, Pieter Harpe, Huijuan, Zhong Jie, Kerong, Tang Qin, Dajie, Zeng Zeng, Wanghua, Miao Jing, Shu Chang, Huang Cong, Bi Yu, Qu Fei, Zhao Duan, Jiansong, Eva, Liu Chi, Meng Zhengjia, Xu Tao and Zhao Yu. Thanks for all good time we spent together on courses, parties or other activities.

Apart from my research work, I’ve also spent a lot of time on cello playing. I would like to thank my cello teacher Anke. I would also like to thank Cees for his piano accompaniment in several performances. Thanks friends in Krashna Musika, especially friends from the cello group. We have played so many concerts together. These are all good memories in my life.

I would like to thank Gina for helping me improve my spoken Dutch. I am grateful to Sarah for her feedbacks on the English text of this thesis.

Finally, I would like to give my deepest gratitude to my family. Thanks Papa and Mama, who always love me, support me, trust me and stimulate me to explore the world in my own way. Thanks my husband Shubin for his love, care and understanding. Thanks my parents-in-law for their support. For my grandparents, they are always living in my heart.

# About the Author

***Zili Yu*** was born in Hangzhou, China, in 1984. She received her B.Sc. degree in Electronic and Information Engineering from Zhejiang University, China in June 2005. She obtained an M.Sc. degree in 2007 from Delft University of Technology, The Netherlands. During her Master's study, her research topic was on the design of precision voltage references. Since 2007, she has been working on her Ph.D. research project, which is designing the front-end electronics for ultrasound transducers for 3D echocardiography. Her research interest is on sensor interface and mixed-signal circuit design.

In her spare time, she likes reading, listening to classical music and playing musical instruments. She is an amateur cellist and plays orchestral/chamber music works.